'ATE VELOCITY DECEPTION AMP

AM-7338/ULQ-21 (V)

Part Number 1611AS722

SYSTRON DONNER MICROWAVE DIVISION

A THORN EMI company

ENGINEERING MANUAL

SOLID STATE VELOCITY DECEPTION AMPLIFIER

AM-7338/ULQ-21 (V)

Part Number 1611AS722

MICROWAVE
DIVISION
SYSTRON
DONNER
A Member of the THORN EMI Group

Contract N00123-87-C-0479
CDRL #B00B

Submitted to:

COMMANDER

PACIFIC MISSILE TEST CENTER

Bldg. 3008, Code 4042.1
Pt. Mugu, CA. 93042

Manual P/N 314441
June 1, 1988

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1.0 INTRODUCTION

Systron Donner Microwave Division designs, develops and manufactures the Solid State Velocity Deception Amplifier (VDA) AM-7338/ULQ-21(V) for Pacific Missile Test Center (PMTC), Pt. Mugu, CA. under Contract Number N0429A-82-C-0306, N00123-84C-0519 and N00R3-87-C-0479. The VDA is small, lightweight, versatile,used as stand-alone or with other jammers. The VDA is a state-of-the-art countermeasures device to replace the AN/DLQ-3C for use in unmanned aerial targets, in manned aircraft and in the AN/ALQ-167 pod. It performs three major functions; an amplifier function, a frequency modulation (FM) function and an amplitiude modulation (AM) function. The VDA replaces four major AN/DLQ-3C assemblies. The TWT Preamplifier, the Radio Transmitter Modulator, the Drone Training Serrodyne Board and the Amplitude Modulation Board. The VDA covers 5.4 to 10.5 GHz, has a minimum output power of 23 dBm, a minimum gain of 50 dB and generates the following ECM modes: Velocity Gate Stealer (VGS), Narrow Band Repeater Noise (NBRN), Random Doppler (RD), Pseudo Random Noise (PRN), Hold Out and Hook (HOH), Multiple Frequency Repeater (MPR), Repeater Swept Amplitude Modulation (RSAM), VGS and RSAM (VGS/), Repeater, Standby, Blinking Pseudo Random Noise (BPRN), Count Down Blink (CDB).

1.1 ENGINEERING MANUAL PURPOSE

This engineering manual provides information to users in engineering areas that are involved in testing and integrating the solid state velocity deception amplifier AM-7338/ULQ-21(V). The manual also provides the information necessary to understand the operating portion as well as the troubleshooting technique and maintenance of the VDA.

1.2 VDA GENERAL PHYSICAL DESCRIPTION

The VDA is constructed in the alumina rectangular box 6"x8"x3.6" with 2 SMA connectors to access to RF input and output connections (See Figure 1.2). All connectors are located on one side of the VDA. An input/output (I/O) 25 pins D-type connector at J6004 to interface to the data entry module or RS-232C Interface Assembly. A multipin connector at J6001 with 22 pins to accept the +28 VDC input power and the deception module remote control logic command. The four NAS1068C08M floating nuts are installed at VDA's bottom plate for easy mounting on the VDA to the ECM system.

1.3 ENGINEERING MANUAL SCOPE

This manual is a technical manual for use by engineering personnel familiar with the technical requirements of the AN/DLQ-3C system. The manual provides the information to operate the VDA as a stand alone unit or interfacing with the remote controller or data entry module. A various assembly included in the VDA system will be described with detailed circuit diagram to show the operating interconnect diagram and schematics.

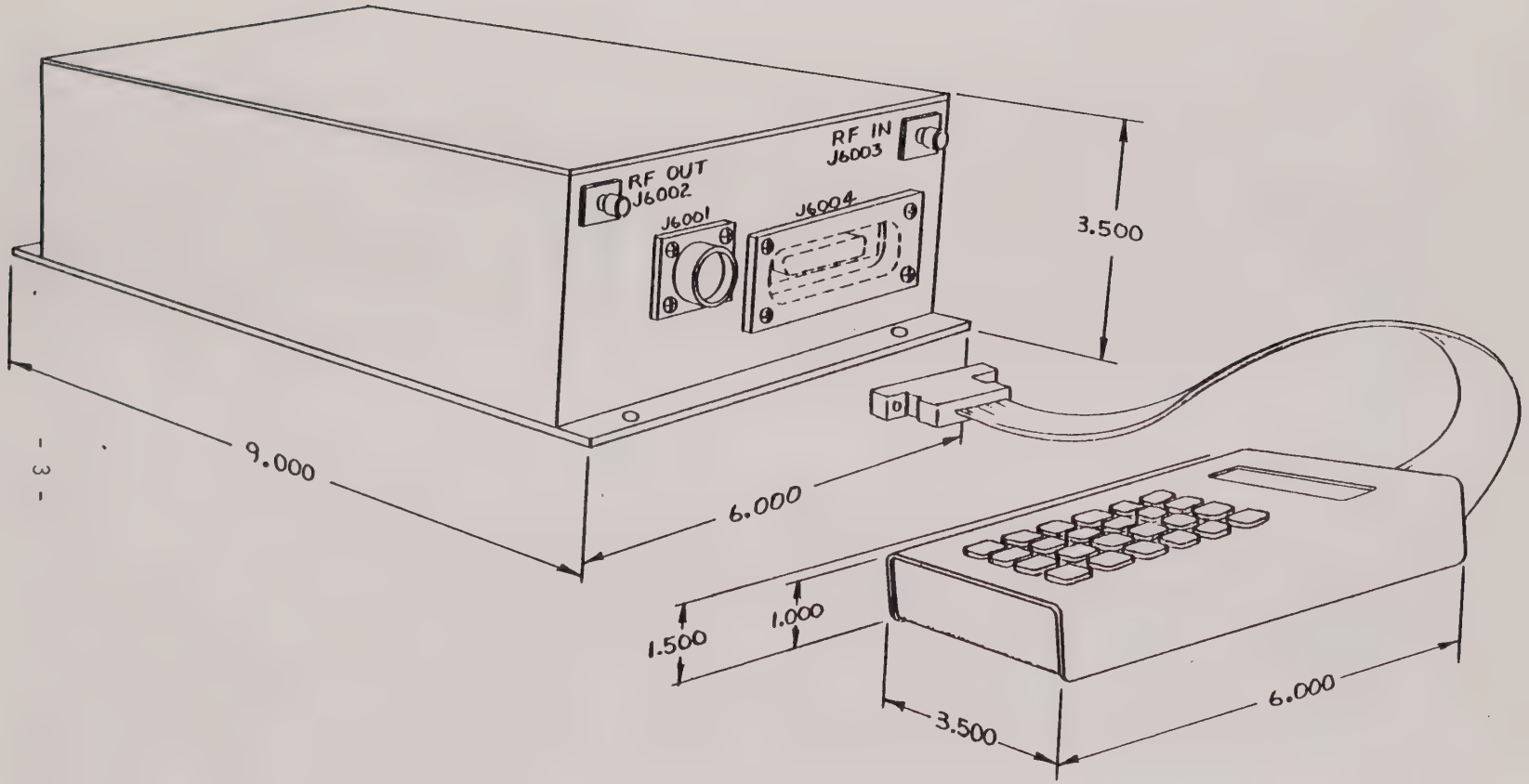


FIGURE 1.2: VDA PHYSICAL DESCRIPTION

2.0 OPERATION

The VDA is operated by applying the prime DC power 28±3VDC to pin 13 of multipin connector J6001 with pin 14 as a ground return. Before turning the DC power on, a data entry module or RS-232C Interface Assembly is connected to I/O port J6004 for VDA parameters entering purpose. For checking the VDA performances of various deception modes, inject an RF signal from stable synthesizer source into RF input port J6003 of the VDA, the RF output port J6003 is then connected to a spectrum analyzer. The step by step instructions are provided on Table 4.0 to guide the operator to program the VDA parameters and modes. All programmed parameters are retained in the VDA after DC power is removed if stored. Once the data entry module is removed, the remote command A,B,C,D at J6001 could be set to select appropriate deception modes.

For using a computer controller to control the VDA, an RS-232C Interface Module is also provided for this function.

2.1 VDA SYSTEM THEORY - (VDA INTENDED FUNCTION)

Figure 2.1 shows the simplified block diagram of the solid state velocity deception amplifier or Serrodynable Frequency Translation System. Serrodyning is provided by a digital phase shifter which consists of five sections of fixed phase shifters that can be switched in and out along the through path in the correct sequence, thereby changing the phase of the RF signal through the assembly in steps. The phase shifter section provides for fixed shift steps of 11.25° and also provides 32 phase steps from 0° to 348.75° (see Table 1.0).

This phase control is provided by a digital signal processor (technique generation assembly). The signal processor generates the necessary

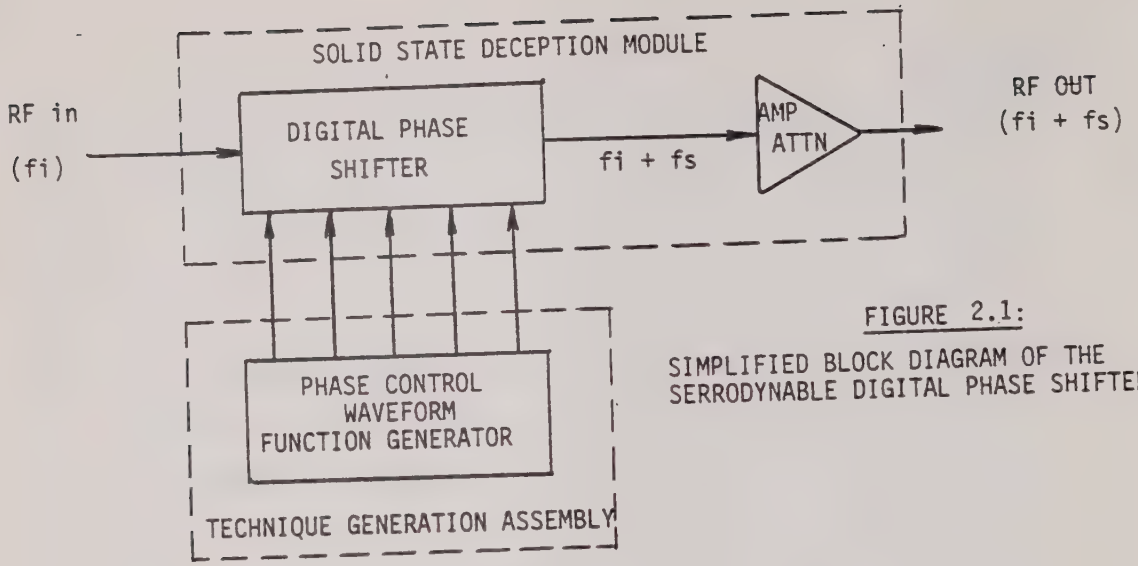


FIGURE 2.1:

SIMPLIFIED BLOCK DIAGRAM OF THE SERRODYNABLE DIGITAL PHASE SHIFTER SYSTEM

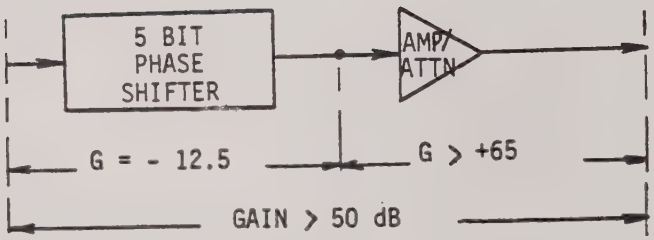


FIGURE 2.2: SYSTEM GAIN DISTRIBUTION

TABLE 1: BINARY CODE vs. PHASE SHIFT

BINARY CODE	PHASE CELLS					PHASE SHIFT
	11.25°	22.5°	45°	90°	180°	
00000						0.00°
00001	X					11.25°
00010		X				22.50°
00011	X	X				33.75°
00100			X			45.00°
00101	X		X			56.25°
00110		X	X			67.50°
00111	X	X	X			78.75°
01000				X		90.00°
01001	X			X		101.25°
01010		X		X		112.50°
01011	X	X		X		123.75°
01100			X	X		135.00°
01101	X		X	X		146.25°
01110		X	X	X		157.50°
01111	X	X	X	X		168.75°
10000					X	180.00°
10001	X				X	191.25°
10010		X			X	202.50°
10011	X	X			X	213.75°
10100			X		X	225.00°
10101	X		X		X	236.75°
10110		X	X		X	247.50°
10111	X	X	X	X	X	258.75°
11000				X	X	270.00°
11001	X			X	X	281.25°
11010		X		X	X	292.50°
11011	X	X		X	X	303.75°
11100			X	X	X	315.00°
11110	X		X	X	X	326.25°
11110		X	X	X	X	337.50°
11111	X	X	X	X	X	348.75°

functions needed for deception jamming mode. The appropriate phase functions are provided by a 5-bit binary code to turn the individual cell on and off in the phase shifter.

The output translated frequency of the digital phase shift section is fed into a GaAs FET amplifier. Figure 2.2 shows the RF system gain distribution. The solid state deception module is capable of 50 dB of gain and power output of +23 dBm minimum at the 1 dB compression point.

2.2 PHYSICAL ARRANGEMENT

The VDA is constructed in one housing with two cavities. One cavity contains the solid state microwave assembly (the two amplifiers and a phase shifter) which locates on the top side of the VDA. The other cavity contains the technique generation, power supply and associated hardness assemblies which locates on the bottom side of the VDA. All RF, I/O connectors locate on one side of the VDA to allow the user access to the cavity. A 22 multipin connector at J6001 is to accept the incoming DC supply +28V$\pm$3VDC and the remote command A,B,C,D. The important test points are also brought out through J6001 for monitor function (See Figure 5.17 for detailed information). An I/O D-type connector at J6004 to interface to the data entry module or computer controller through an interface module assembly.

Table 2: VDA Frequency Modulation Section Specifications

Characteristic	Specified Value
Frequency Range	5.4 to 10.5 GHz
Carrier Suppression (within ±50 kHz of Carrier)	-20 dB minimum
Maximum FM Deviation	127.5 kHz minimum
Harmonic and Spurious Emissions	-20 dB minimum
Spectral Purity (within ±10% kHz of Carrier)	-45 dB minimum

Table 3: Function Generator Section Mode Parameter Specifications

Mode	Characteristic	Specified Value
VGS	Velocity Gate Stealer	
	Maximum Frequency Deviation	500 Hz to 127.5 KHz
	Minimum Frequency Deviation	20 Hz maximum
	Frequency Stability	
	500 Hz to 10 KHz Deviation	±10%
	10 KHz to 127.5 KHz Deviation	±5%
	Dwell Time	50 ms to 5 seconds
	Walk Time	100 ms to 25.5 seconds ± 10%
	Walk Linearity	Linear or Parabolic
	Direction	Positive or Nevative
	Translation Loss	
	20 Hz to 50 kHz Deviation	4 dB maximum
	50 kHz to 127.5 kHz	9 maximum
NBRN	Narrow Band Repeater Noise	
	Maximum Frequency Deviation	125 Hz to 32 kHz
	Minimum Frequency Deviation	20 Hz maximum
	Frequency Stability	
	125 Hz to 5 kHz Deviation	±10%
	5 kHz to 32 kHz Deviation	±5%
	Walk Time	Alternating positive and negative every 1 ms. At the beginning of each 50 ms walk, direction will alternate.
	Amplitude Modulation Frequency	450 Hz ±10%
	Amplitude Modulation Duty Cycle	40%
	Translation Loss	3 dB maximum
RD	Random Doppler	
	Maximum Frequency Deviation	100 Hz to 25.5 kHz
	Minimum Frequency Deviation	100 Hz maximum
	Frequency Stability	
	100 Hz to 5 kHz Deviation	±10%
	5 Khz to 25.5 KHz Deviation	±5%
	Duration Period	200 ms to 20 ms
	Direction	Alternating positive and negative every duration period.
	Translation Loss	3 dB maximum

Table 3
Page Two

Mode	Characteristic	Specified Value
PRN	Pseudo Random Noise	
	Bandwidth	50 Hz to 5 KHz (programmable thru RD mode)
	Translation Loss	≤ 3 dB
BPRN	Blinking Pseudo Random Noise	
	Bandwidth	50 Hz to 5 kHz (programmable thru RD mode)
	Translation Loss	≤ 3 dB
	AM Frequency Range	0.1 to 22.5 Hz and 1/100 of the programmable MFR frequency
RSAM	Repeater Swept Amplitude Modulation	
	Start Frequency	5 Hz to 1275 Hz
	Stop Frequency	5 Hz to 1275 Hz
	Sweep Ratio	1:1 to 10:1
	Sweep Time	50 ms to 12.75 seconds
	Duty Cycle	10% to 90%
MFR	Multiple Frequency Repeater	
	Frequency Range	10 Hz to 2250 Hz
	Duty Cycle	10% to 90%
HO&H	Hold Out and Hook	
	Maximum Frequency Deviation	500 Hz to 127.5 kHz
	Minimum Frequency Deviation	20 Hz maximum
	Frequency Stability	
	500 Hz to 10 kHz Deviation	±10%
	10 kHz to 127.5 kHz Deviation	±5%
	Dwell Time	50 ms to 5 seconds
	Walk Time	100 ms to 25.5 seconds
	Hold Time	100 ms to 25.5 seconds
	Walk Linearity	Linear or Parabolic
	Direction	Positive or Negative
	Direction	
	Translation Loss	
	20 Hz to 50 Hz Deviation	4 dB maximum
	50 kHz to 127.5 kHz Deviation	9 dB maximum

Table Three
Page Three

Mode	Characteristic	Specified Value
VGS	VGS with Angle or VGS & RSAM	
	Maximum Frequency Deviation	500 Hz to 127.5 kHz
	Minimum Frequency Deviation	20 Hz maximum
	Frequency Stability	
	500 Hz to 10 kHz Deviation	+10%
	10 kHz to 127.5 kHz Deviation	+5%
	Dwell Time	500 ms to 5 seconds
	Walk Time	100 ms to 25.5 seconds
	Walk Linearity	Linear or Parabolic
	Direction	Positive or Negative
	Translation Loss	
	20 Hz to 50 kHz Deviation	4 dB maximum
	50 kHz to 127.5 kHz Deviation	9 dB maximum
	RSAM Insertion Point	3 kHz to 127.5 kHz
CDB	Count Down Blink	
	Frequency Range	.01 to 22.5 Hz (1/100 MFR frequency)
	Duty Cycle	10% to 90%

2.3 OPERATION MODES

2.3.1 GENERAL

The deception module has the remote control capability to command the following modes:

a. Velocity Gate Stealer (VGS)
b. Narrow Band Repeater Noise (NBRN)
c. Random Doppler (RD)
d. Pseudo Random Noise (PRN)
e. Velocity Gate Stealer (VGS) and Repeater Swept Amplitude Modulation (RSAM)
f. Hold Out and Hook (HO&H)
g. Repeater Swept Amplitude Modulation (RSAM)
h. Multiple Frequency Repeater (MFR)
i. Repeater
j Blinking PRN(BPRN)
k. Standby (STBY)
l. Count Down Blink (CDB)

All modes of parameters are programmed by using the software command via the data entry module or RS-232C interface assembly to the computer controller. No mechanical adjustments are needed.

2.3.2 DESCRIPTION OF DECEPTION JAMMING MODES

The VDA's twelve ECM techniques are described below and their specifications are listed in Table 2 and 3.

2.3.2.1 VELOCITY GATE STEALER (VGS)

The VGS mode is generated by phase shifting the input signal to produce a slowly changing, false frequency. The offset is initially held at zero before being slowly swept out to the maximum offset, where it is rapidly snapped back to zero offset. The false signal can be translated either upward or downward, linear or parabolic in frequency.

2.3.2.2 NARROW BAND REPEATER NOISE (NBRN)

The NBRN is generated by phase shifting the input frequency with a rapidly swept, sawtooth waveform. The translation frequency is swept rapidly at a 50 msec rate, from about 20 Hz to the maximum deviation frequency which has been preset. While the frequency is being swept, the direction of the frequency translation is alternately switched between positive and negative. A fixed amplitude modulation is also used with the serrodyning to add more lines to the RF Spectrum.

2.3.2.3 RANDOM DOPPLER (RD)

The RD mode is generated by translating the input frequency by a randomly selected fixed amount and holding it for a set period before moving the frequency to the next translated value. The translated frequency is also alternated between a positive and negative frequency shift with each successive period. In RD mode, both the hold time and maximum translation frequency are adjustable.

2.3.2.4 PSEUDO RANDOM NOISE (PRN)

The PRN is generated by phase shifting the input frequency by a continuously varying amount. A data shift logic circuit is implemented to produce smearing effect. The amount of deviation is determined by random doppler time.

2.3.2.5 VELOCITY GATE STEALER AND REPEATER SWEPT AMPLITUDE MODULATION (VGS$\frac{1}{2}$)

The VGS$\frac{1}{2}$ mode is the combination of VGS and RSAM where a standard VGS is run with RSAM added after an adjustable delay.

2.3.2.6 HOLD OUT AND HOOK (HOH)

The HO&H is quite similar to VGS in that it is generated by phase shifting the input signal to produce a slowly changing, false frequency. The offset is initally held at zero before being slowly swept out to the maximum offset, where it is held for an adjustable period prior to being rapidly snapped back to zero offset. The false signal can be translated either upward or downward, parabolic or linear in frequency.

2.3.2.7 REPEATER SWEPT AMPLITUDE MODULATION (RSAM)

The RSAM mode is generated by amplitude modulating the signal at a frequency which is linearly varied in a sawtooth fashion between preset frequency limits while the duty factor is held constant.

2.3.2.8 MULTIPLE FREQUENCY REPEATER (MFR)

The MFR mode is generated by applying a pulse amplitude modulation, with a programmable frequency and duty cycle, to the amplified input signal.

2.3.2.9 REPEATER (RPTR)

In the RPTR mode, the VDM serves as an amplifier for other AN/DLQ-3 assemblies. No internal waveforms are generated as external modulation is applied.

2.3.2.10 BLINKING PSEUDO RANDOM NOISE (BPRN)

The BPRN is the combination of PRN and MFR where a standard PRN is run with MFR is added at a programmable rate 1/100 of MFR.

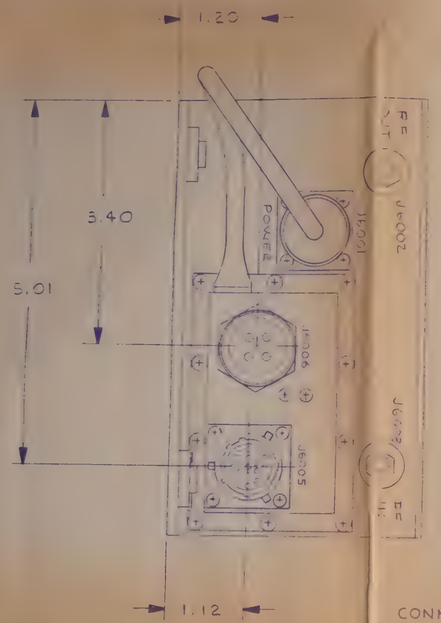
2.3.2.11 STANDBY (STBY)

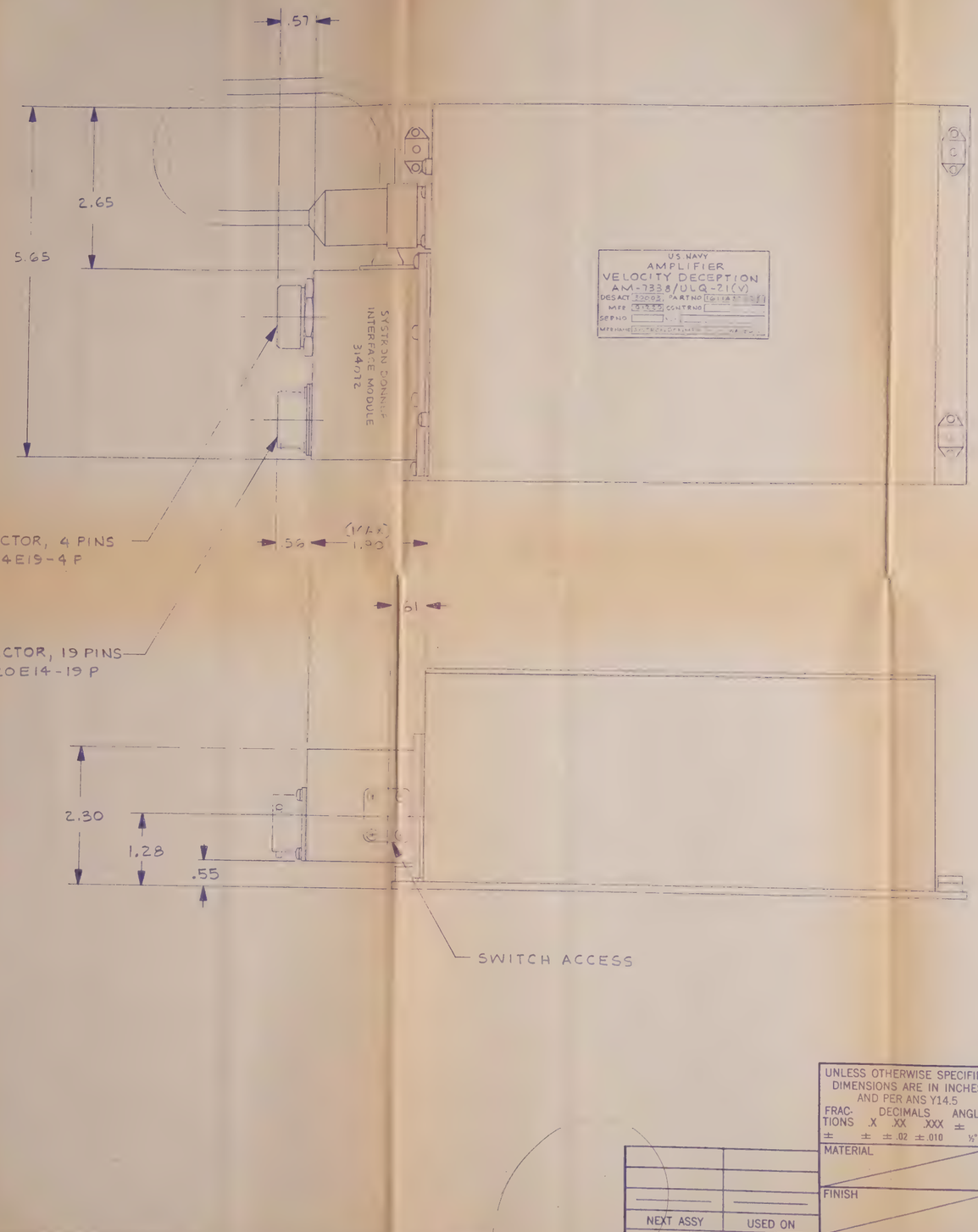
The STBY mode is generated by triggering the MFR circuitry with a TTL high level to reproduce a non-serrodyne output with full attenuation.

2.3.2.12 COUNT DOWN BLINK (CDB)

This CDB mode is quite similar to MFR mode except the CDB frequency is 1/100 of MFR frequency.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SH 1		





US NAVY
AMPLIFIER
VELOCITY DECEPTION
AM-7338/ULQ-21(V)
DESACT 22003, PARTNO [illegible]
MFR 01295 CONTRNO
SERNO
MFRNAME [illegible]

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
AND PER ANS Y14.5
FRACTIONS ± | DECIMALS .X ± .1, .XX ± .02, .XXX ± .010 | ANGLES ± ½°
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.
DR BY
CHK BY
APPROVED BY

SYSTRON DONNER MICROWAVE DIVISION
CORPORATION
[illegible]

OUTLINE DRAWING, VELOCITY DECEPTION MODULE

SIZE	CODE IDENT NO.	DWG NO.
D	01220	OD312068-01

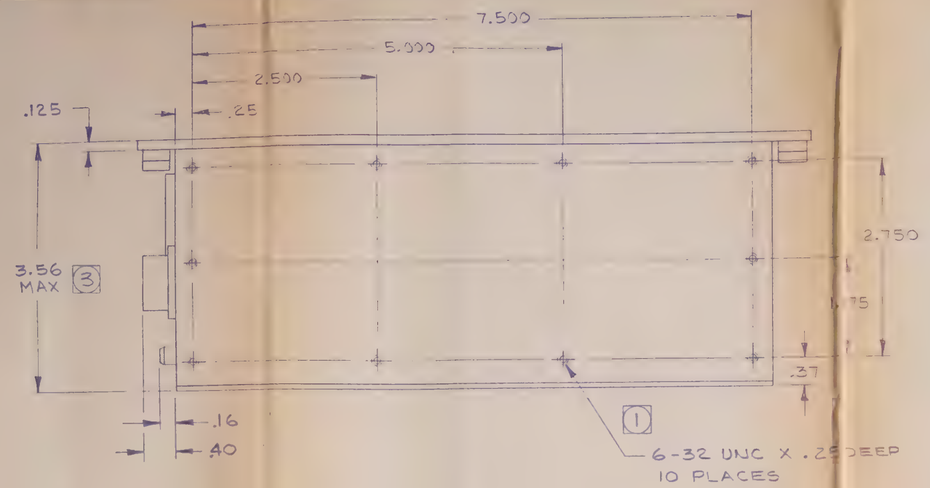
SCALE —
SHEET 2 OF 2

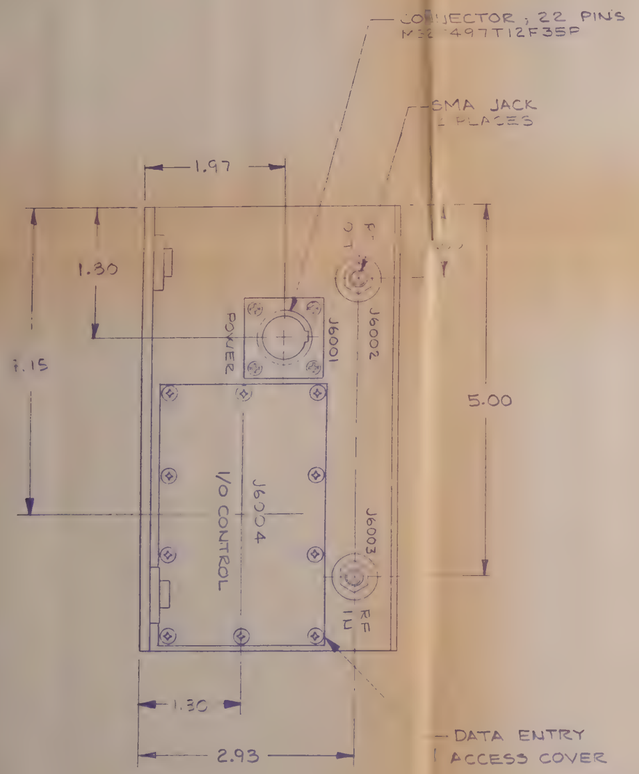
O.T.E.R.I.C.H. POST C. EARP N.Y. 11020

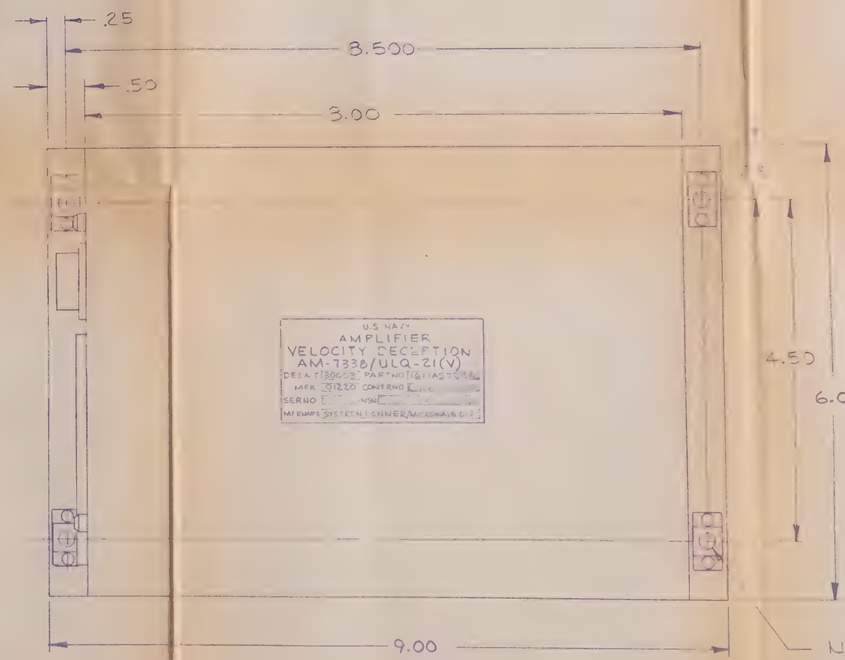
NOTES

1. THIS IS AN ALTERNATE MOUNTING HOLE PATTERN IT IS ON BOTH SIDES OF THE UNIT. IF ONE OF THESE SIDES ARE USED AS THE MOUNTING SURFACE ONE OF THE OTHER MOUNTING SURFACES SHOULD BE USED TO BALANCE THE UNIT.
2. FOR OUTLINE OF OPTIONAL INTERFACE MODULE SEE SHEET 2
3. DIMENSION DOSE NOT INCLUDE IDENTIFICATION PLATE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL PER EO 18364	8/24/87	JS
	B	REV PER EO 18377	9/14/87	JS
	C	REV PER EO 18404	9/21/87	JS
	D	REV PER EO 18414	9/23/87	JS
	E	REV PER EO 18424	10/1/87	JS
	F	REV PER EO 18463	12/1/87	JS







SEE SEPARATE PARTS LIST PL312068-01

	VDM
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND PER ANS Y14.5
FRACTIONS ± | DECIMALS .X ± .1 .XX ± .02 .XXX ± .010 | ANGLES ± ½°

MATERIAL SEE PL312068-01

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY MK Conner 7/15/87
CHK BY [illegible] 9/3/87
APPROVED BY

SYSTRON DONNER MICROWAVE DIVISION
CORPORATION
8888 DENBIGH ST. VAN NUYS, CALIFORNIA 91411

OUTLINE DRAWING, VELOCITY DECEPTION MODULE

SIZE	CODE IDENT NO.	DWG NO.
D	01220	OD312068-01

SCALE —

SHEET 1 OF 2

3.0 DETAILED PHYSICAL DESCRITPION OF THE VDA

The detailed outline description of the VDA is shown in the D size attached outline drawing OD 312068-01 Sheet 1 & 2. The four 8-32 floating nuts were added for easy mounting of the VDA to the ECM systems. The technique generation assembly (digital and analog PCB's) and power supply assembly are located in the bottom compartment of the VDA. The phase shifter and amplifier assemblies are in three separate housings and located on the top compartment of the VDA. They are cascaded through the semi-rigid cable from RF input to output ports with SMA connector at both ends.

3.1 PHASE SHIFTER CIRCUIT DESCRIPTION

The phase shifter or frequency modulation section provides the phase modulation necessary to serrodyne the input frequency. The commonly used serrodyning technique of placing a linear sawtooth voltage on a helix requires a TWT. Serrodyning is a technique in which an RF signal is phase modulated at a rate of $\frac{d\phi}{dt}$ produce an output frequency W_o in which the input W_i is shifted by the phase modulation.

The output signal is given by the equation:

$$W_o = W_i + \frac{d\phi}{dt}$$

In the VDA, the $\frac{d\phi}{dt}$ sawtooth phase modulation is replaced with the 5 bit binary word, $\frac{d\phi}{dt}$ is advanced in 32 discrete steps of 11.25° each per cycle of code. Total phase shift is 0° to 348.75° in 11.25° steps (See Table 1.0).

The phase shifter circuitry is comprised of five separate diode phase shift cells: 11.25°, 22.5°, 45°, 90° and 180° (See Figure 3.1.1.A).

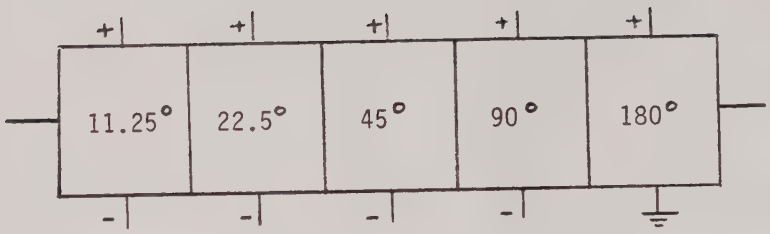


Figure 3.1.1.A: 5-Bit Phase Shifter Configuration

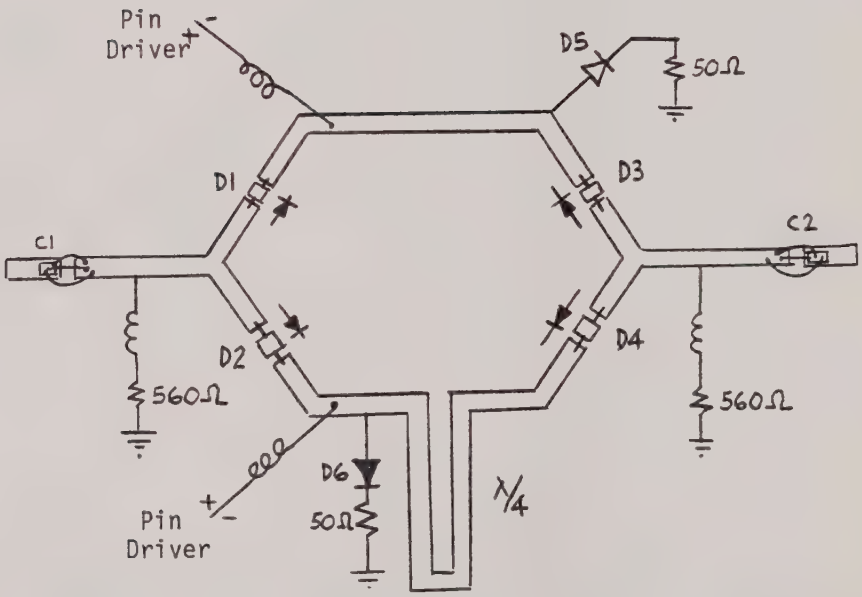


Figure 3.3.1.B: Schematic of Typical Phase Cell

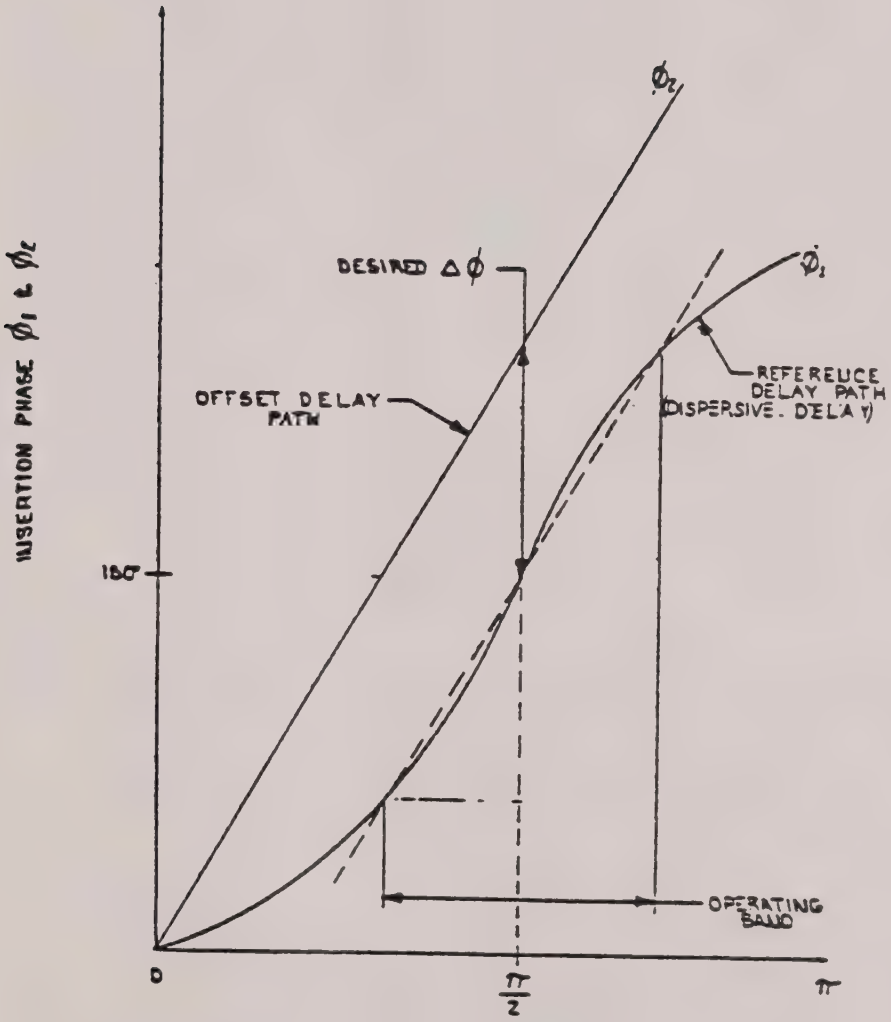


FIGURE 3.1.2

SCHEMATIC -- TYPICAL PHASE CELL

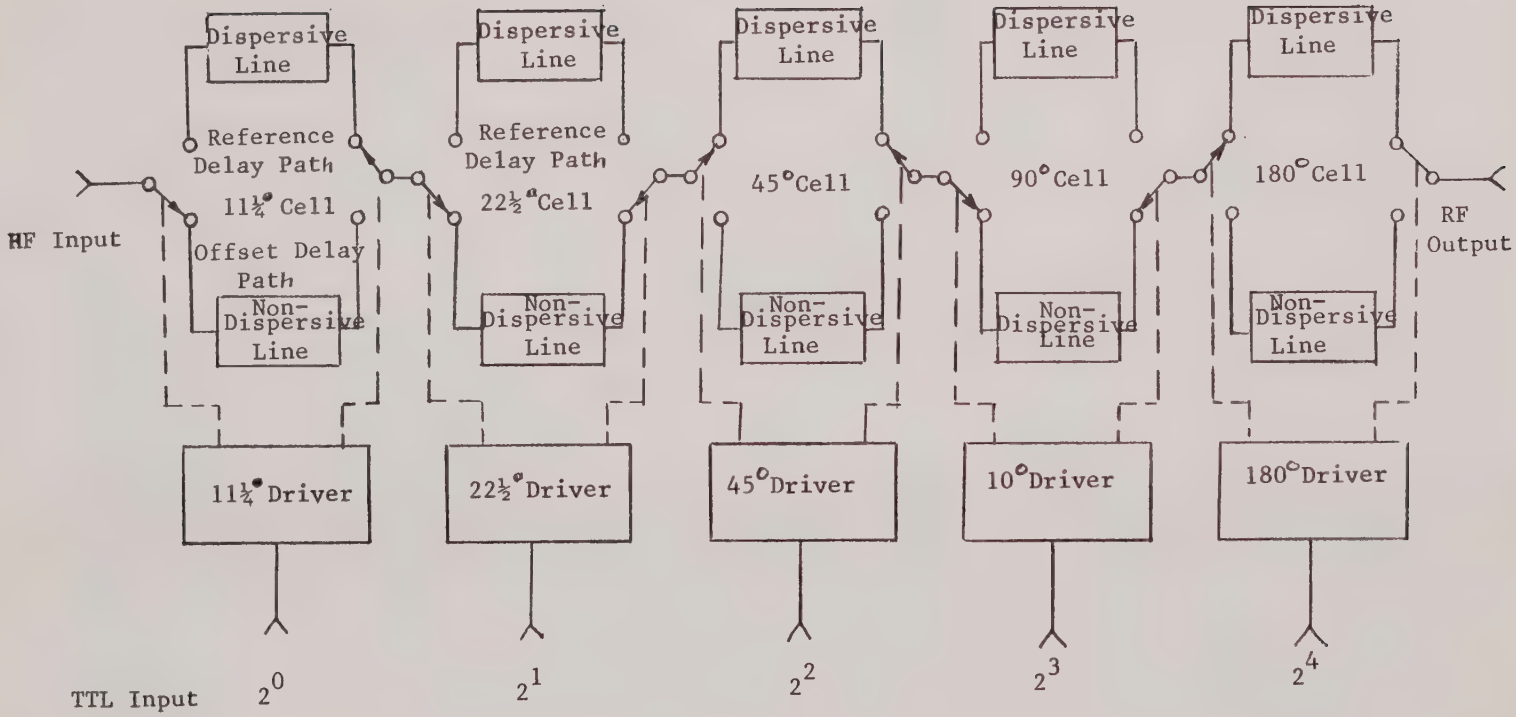


FIGURE 3.1.3

MODE DIAGRAM DIGITAL RF PHASE SHIFTER

The phase shift cells are constructed on microstrip using a Schiffman type delay line to cover up to an octave bandwidth. A Schiffman phase shifter element consists of a pair of alternately switched lines, one of which is a dispersive line section containing a quarter wave coupled transmission line shorted on one end and on the other a non-dispersive line (transmission line) with a linear phase shift slope with frequency. To achieve a constant phase shift over the desired frequency band, the differential phase shift ($\Delta\phi$) between the non-dispersive and dispersive section is compared over the specified bandwidth. The chip capacitors and resistors are used as DC blocks and bias circuit elements. For a $\frac{\lambda}{4}$ coupled transmission line section the phase shift is given by:

$$\phi = \cos^{-1} \frac{p - \tan^2\phi}{p + \tan^2\phi} \qquad (3.1.1)$$

where $p = \frac{Zo_e}{Zo_o}$ ratio of even/odd impedance of the coupled transmission line

ϕ = the electrical length of the coupled lines

For the non-dispersive part line (reference path),

$$\phi_2 = k\,\phi$$

where k is the ratio of the non-dispersive length to the dispersive length. The differential phase shift is then:

$$\Delta\phi = \phi_2 - \phi_2 = k8 - \cos^{-1} \frac{p - \tan^2\phi}{p + \tan^2\phi} \qquad (3.1.2)$$

Figure 3.1.2 shows a typical plot of the phase shift conditions described by Equation 3.1.2.

The dispersive line always introduces an insertion phase of 180° at mid-band. By adjusting the coupling ratio $\frac{Zo_e}{Zo_o}$ of the coupled line section (Schiffman delay element), the phase slope or phase change vs. frequency of the dispersive transmission line can be made to track that of the non-dispersive line with the exception that a fixed phase offset at mid band is introduced in the dispersive line. The resultant is a broad band phase shifter with very little phase error over the desired frequency band. Note that the desired output phase shift in Figure 5.2 is represented by $\Delta\phi$, which is the difference in phase between the dispersive and non-dispersive delay line.

For example, the 90° phase shift cell must contain a 270° non-dispersive line at mid band in order to obtain the desired 90° offset. By optimizing the $\frac{Zo_e}{Zo_o}$ ratio, the phase slopes of both lines are almost equal over an octave bandwidth.

Amplitude variations due to phase shifter element switching contributes AM sidebands, which in turn will increase spurious sideband levels. The matched PIN diode pairs are used to minimize the AM effects. The various signal paths have almost equal losses except for transmission line and mismatched diode losses (Figure 3.1 showing the cell block diagram). These differences are controlled in the microstrip construction so that the peak amplitude variation is less than $\pm$ 1 dB for any combination of the phase shift elements. To minimize size, a

high ε_r dielectric substrate (alumina) is used. All cells are similar except for the coupling ratio of the Schiffman coupled line section and the length of the non-dispersive transmission line.

The configuration of the phase shift cell offers minimal insertion loss variation when switching between the reference and offset delay transmission lines due to the matched diode pairs (D_1, D_2) and (D_3, D_4) and minimal transmission line lengths connecting each SP2T switch. Note that the configuration of the Schiffman phase shifter on microstrip lends itself to fine tuning of its phase shift characteristics by using a dielectric block to reduce the coupling between the lines. The phase shifter is hermetically sealed to protect the beam lead diodes. The block diagram of the complete modulator system was given in Figure 3.1.3.

3.2 AMPLIFIER CIRCUIT DESCRITPION

The block diagram of the VDA's GaAs FET amplifier is shown in Figure 3.2. The amplifier contains balanced gain stages, a temperature compensation circuit for gain control over temperature, and two sections of pin attenuator for modulation purpose. The gain, attenuator stages are constructed on alumina substrates which are eutectically attached to stainless steel carriers. These stages are assembled into a heremetically sealed housing. Hermeticity is ensured by epoxy sealing the cover of the housing and soldering of all glass-to metal feedthrus and connectors.

Table 3.2 lists the electrical performance specifications for the amplifier. Each gain stage nominally provides 8.5 dB of gain. Temperature compensation stage is used in order to maintain the RF output level

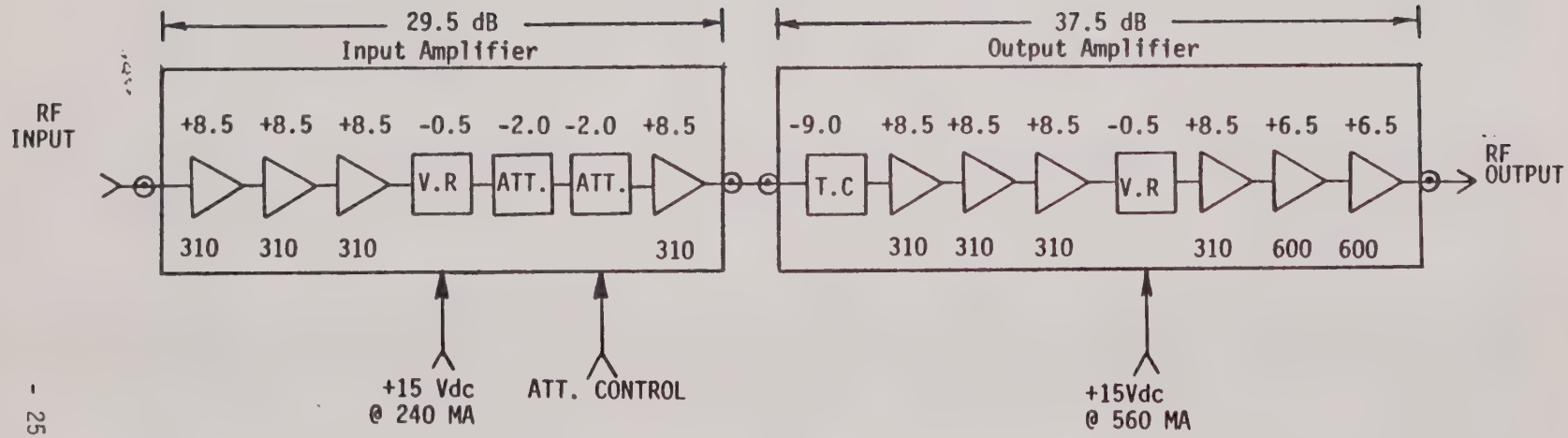


FIGURE 3.2.: Block Diagram of 5.4 - 10.5 GHz GaAs FET Amplifier

TABLE 3.2

ELECTRICAL SPECIFICATION

GaAs FET AMPLIFIER

FREQUENCY RANGE:	5.4 to 10.5 GHz
NOISE FIGURE:	6.0 dB typical
VSWR:	2.0:1 in/out
OUTPUT POWER:	+23 dBm at 1 dB gain compression point
GAIN:	65 dB minimum
TEMPERATURE RANGE:	-45° to +80°C
DC POWER:	+15 Vdc @ 240 mA nominal
	+15 Vdc @ 560 mA nominal

well within a gain window over a specified temperature range of -45° to +80°C. Typically, the gain variation per stage is 0.015 dB/°C. The temp-comp stages utilize a balanced PIN attenuator controlled by a thermistor circuit that cancels the gain variation of the amplifier over temperature.

The temperature compensation circuit consists of a matched pair of PIN diodes used in a balanced configuration to compensate for gain variations of the amplifier from ambient temperature. The attenuation is controlled by a thermistor circuit which operates the circuit at minimum attenuation at high temperature. The attenuation is gradually increased as the temperature decreases. The uncompensated amplifier gain variation per stage is typically -0.015 dB/°C. For instance, the gain variation for an 8-stage ampilfier is expected to be 15 dB from -45° to 80°C. The temp-comp circuit reduces this to 5.6 dB max (gain variation of amplifier over temperature is 60 $\pm$ 2.8 dB).

The balanced approach is realized by using Lange couplers which provide isolation from the highly reflective PIN diode during attenuation. The matched PIN diodes are used to ensure low VSWR's and a flat freqency response over the entire attenuation range.

The thermistor is set to linearly compensate for the gain variation. Since at the temperature extremes the gain variation no longer behaves linearly, perfect gain compensation is not possible. In practice, the temperature compensation circuit reducesthe gain variation by 50 percent minimum.

The built-in attenuator circuit is used in the amplifier assembly to generate the amplitude modulation for the STBY, MFR, NBRN, VGS & RSAM, BPRN, CDB deception modes. The 60 dB Attenuator consists of two attenuator stages controlled by a single driver switch. A pair of shunt diodes in a balanced configuration provides 30 dB attenuation, and by cascading two attenuator stages, 60 dB of attenuation is possible. The attenuator is controlled by a single switch driver with TTL inputs and a switching speed of 100 ns.

3.3 TECHNIQUE GENERATION ASSEMBLY (ANALOG/DIGITAL SIGNAL PROCESSOR)

The technique generation assembly is an integral part of the solid state deception module. (Figure 3.3). It is used to generate specific functions with respect to time which are used to perform frequency translation and amplitude modulation. The specific hardware blocks to generate these functions are:

- Microcomputer Hardware
  1. Microprocessor, PROM
  2. NOVRAM, RAM
  3. Data entry module, RS232C Interface Assembly
- Programmable Frequency Translation Hardware
  4. Linear ramp Hold out and Hook function of type Y=Kx+C
  5. Parabolic ramp function of the type $Y=K\ 10^{X}$
  6. Random voltage sequencer for RD
  7. Voltage sequencer for NBRN, BPRN
  8. Random sawtooth frequency for PRN
  9. Variable gain amplifier
  10. Voltage to frequency converter
  11. Frequency translation driver

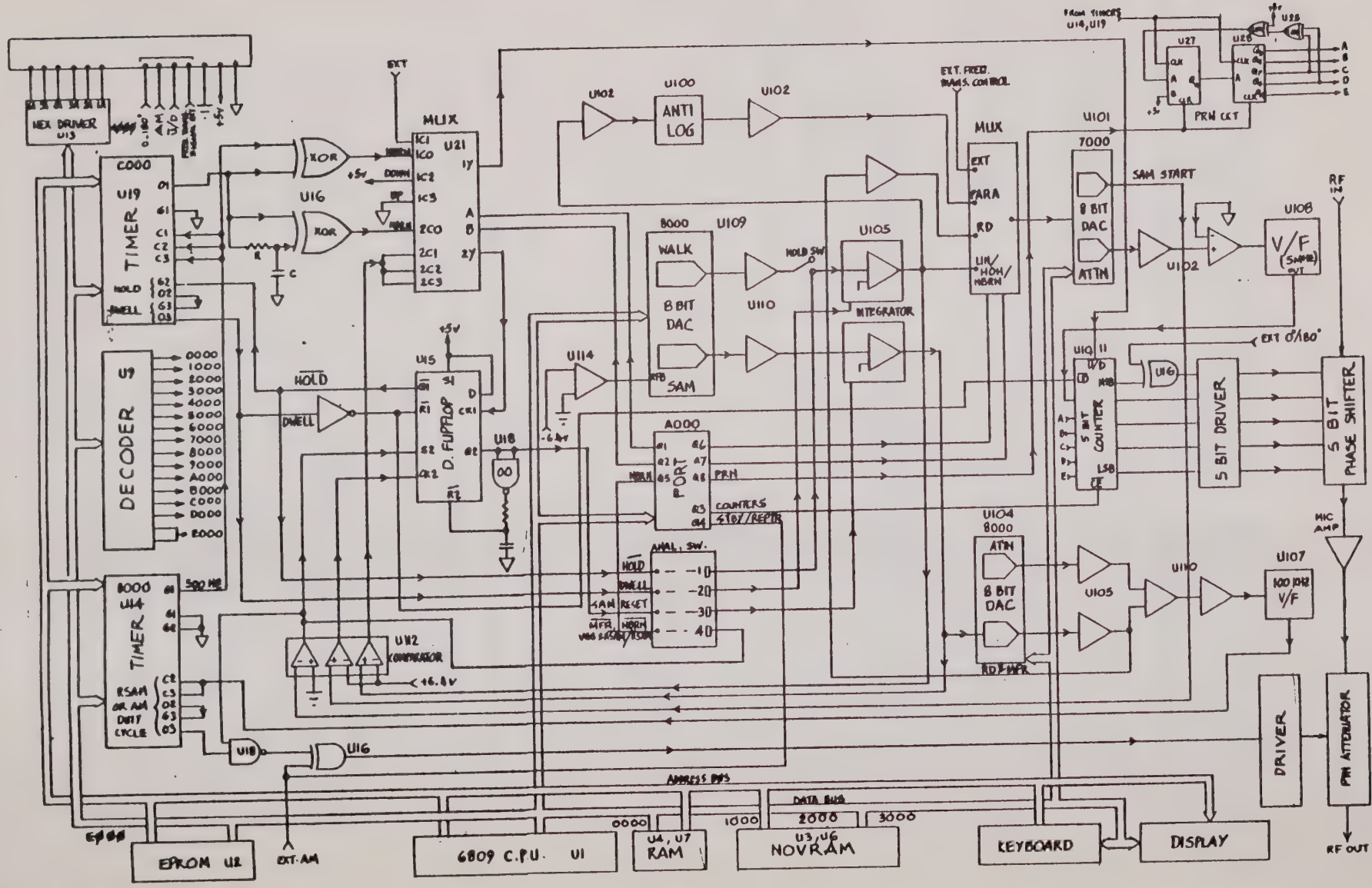


Figure 3.3 Detail Block Diagram of Solid State Deception Module

- Programmable Amplitude Modulation Hardware

  12. Swept voltage generator for VGS + RSAM and RSAM

  13. Single voltage generator for MFR, CDB

  14. External control signals

3.3.1 MICROPROCESSOR, PROM (U1, U2)

The System uses a 8 bit microprocessor unit MC 6809 for setting and control of function parameters. The program for the systems is stored into a 8K x 8UV erasable PROM. The program initializes all hardware to the parameters currently in the parameter registers located in the NOVRAM.

3.3.2 NOVRAM & RAM (U3, U6 & U4, U7)

Flexible programming of parameters is achieved by using NOVRAM. The main advantage of these IC's is the capability of retaining parameters even after power is removed. The NOVRAMS incorporate the advantage of both static RAM and EEPROM. The RAM section is used in real time without using valuable PROM life cycles (10,000/life). The parameters in the RAM can be copied into the PROM and the RAM section erased. Two RAM's of 256X4 memory are used as a scratch pad to store other parameters and do various math calculations.

3.3.3 DATA ENTRY MODULE AND RS-232 INTERFACE ASSEMBLY

The data entry module and RS-232 Interface Assembly provide a means for setting parameters by either Keypad or remote programming. The detailed circuit description is described in Section 3.5 and 3.6 of this manual.

3.3.4 LINEAR WAVEFORM GENERATOR FOR VGS AND HOLDOUT & HOOK (HO&H)

The hardware circuit to generate the linear waveform generator for VGS

and HO&H is shown in Figure 3.3.4.a and b. The multiplying DAC generates the output V_i at TP106 by the following equation:

$$V_i = A_o \; V_{Ref} \tag{3.3}$$

where $A_o = \frac{256}{N}$, V_{Ref} = 0.048V at TP105, N = programmable values from the DAC, $2^8 = 256$ from the DAC

Hence $$V_i = \frac{256}{N} \; V_{Ref} \tag{3.4}$$

An integrating network is implemented to generate a constant amplitude (0.6.4v) ramp function. The relationship between the integrator output and the charging current is defined by:

$$V_o = \frac{1}{C_{110}} \int_0^{\Delta t_w} idt = \frac{1}{C_{110}} i \; \Delta t_w \tag{3.5}$$

where Δt_w = walk time, $i = \frac{Vi}{R_{152}}$, C_{110} = charging capacitor, R_{152} = input resistor, V_o = the voltage output at TP107

$$\Delta t_w = \frac{V_o C_{110}}{i} = \frac{V_o R_{152} C_{110}}{V_i} \tag{3.6}$$

Substitute equation (3.4) to equation (3.6):

$$\Delta t_W = N \frac{V_o \; R_{152} C_{110}}{256 \; V_{Ref}} \tag{3.7}$$

Where V_o = 6.4v, R_{152} = 178K, C_{110} = 1 μ f, V_{Ref} = 0.048v. The walk time Δt_w is directly proportional to the charging capacitor C_{110}, input resistor R_{152}, output voltage V_o, reference voltage V_{Ref} and progammmable value N of the 8 bit DAC.

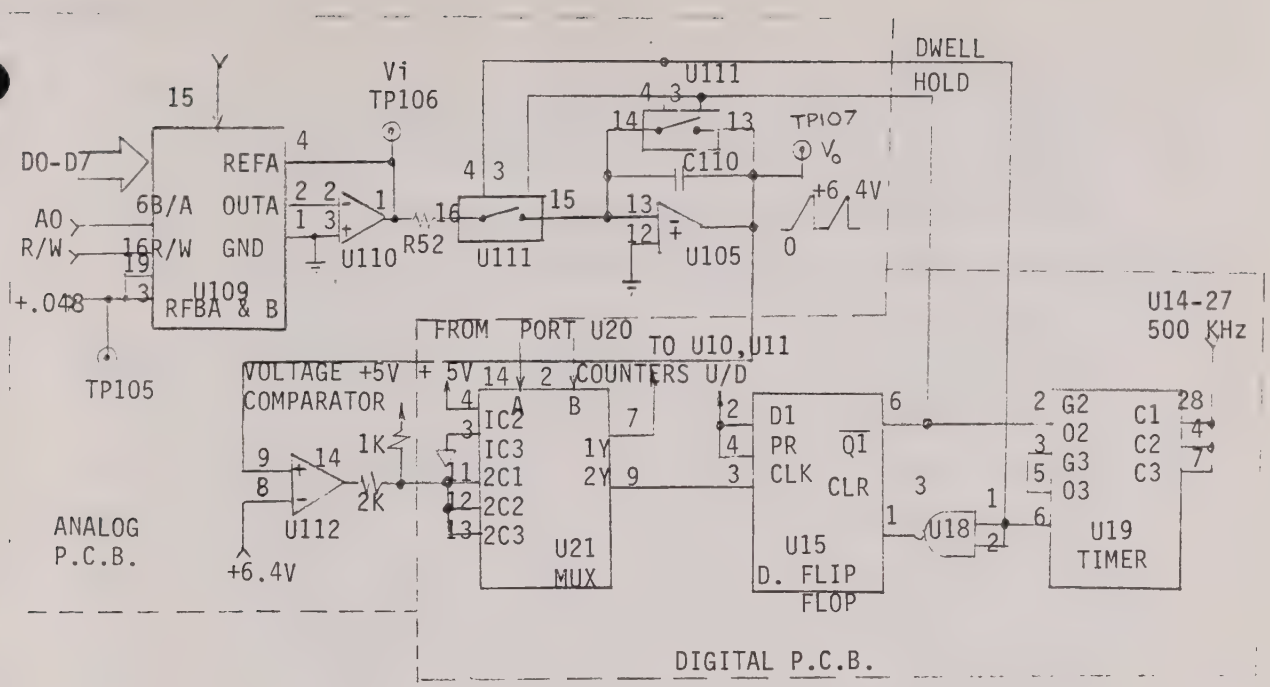


FIGURE 3.3.4.a: RAMP GENERATOR CIRCUITRY FOR VGS & HOH

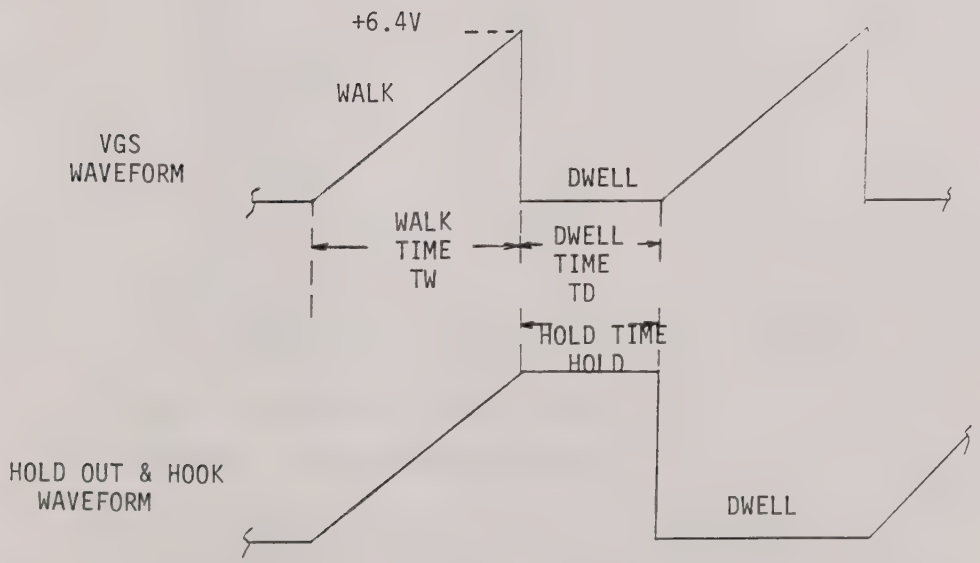
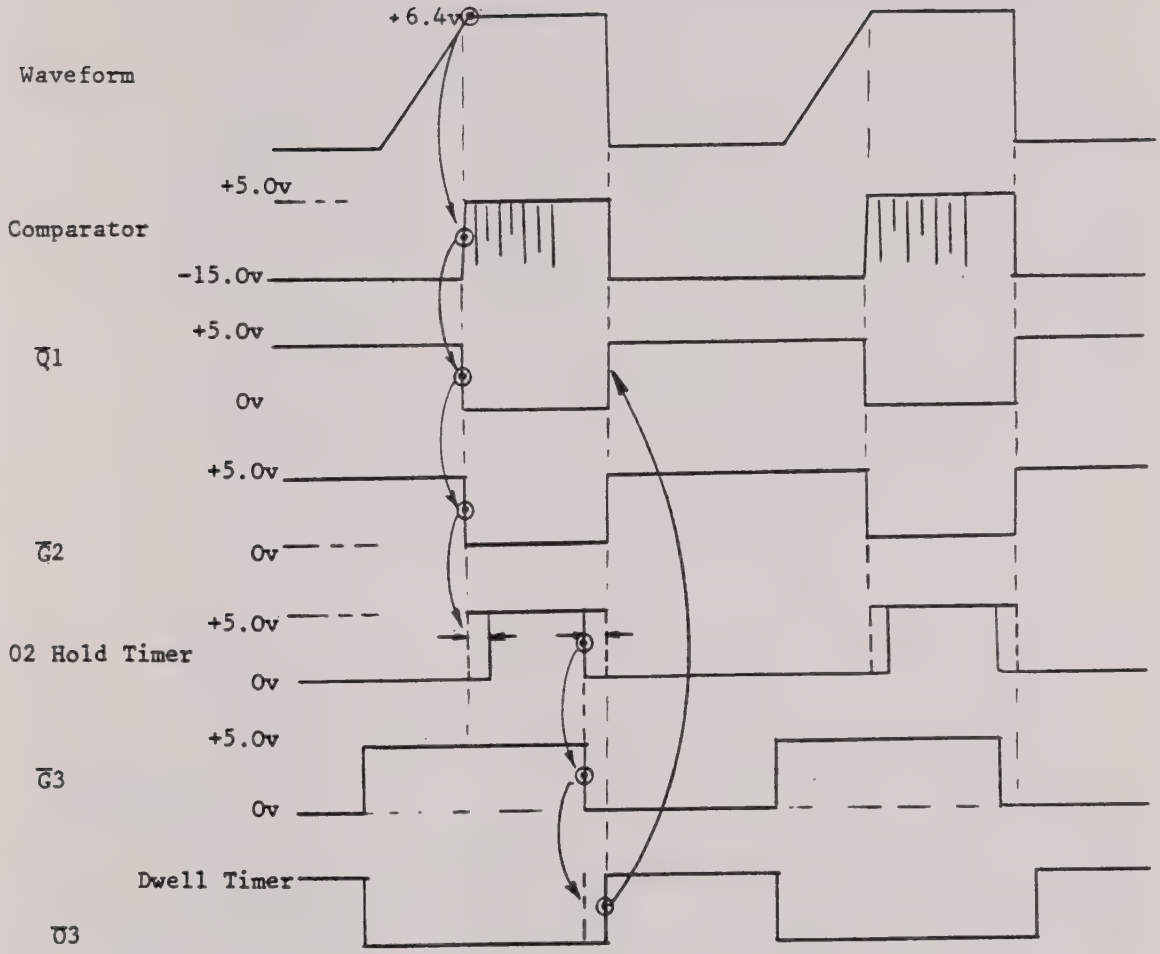


FIGURE 3.3.4.b: BASIC WAVEFORMS FOR VGS & HOH

Since V_o, R_{152}, C_{110} and V_{Ref} are fixed values, the value of N is programmable, so that the minimum ramp time is 0.1 second and the maximum ramp time is 25.5 seconds at maximum amplitude of 6.4 volts. The actual timing of VGS and HO&H waveform is shown in Figure 3.3.4.c.

The comparator U112 compares the ramp voltage V_o to a preset reference voltage of 6.4 volts, when the ramp reaches 6.4 volts, the comparator output changes state and creates a trigger pulse to the clock input of a D-flip flop U15 through the multiplexer U21. On receiving the clock input pulse, Q1 in going low will trigger G2 input of the timer which in turn sets off the HOLD timer output O2 high for the programmed period. It also opens up the HOLD switch in the analog switch: U111. This stops the supply current to the integrator resulting in a steady output voltage. At the end of the HOLD period, O2 in going low triggers G3 of timer. This starts the DWELL time O3, whose pulse remains high for the programmed dwell period. The high pulse goes to the DWEll switch of the analog switch which in turn shorts out the feedback capacitor of the integrator resulting in DWELL time. Also, as O3 goes high, the pulse is inverted and clears the input of the flip flop. Hence Q1 goes high shutting the HOLD switch. Now the waveform is ready to ramp again at the moment the dwell ends. The timing diagram is shown in Figure 3.3.4b. Both VGS and HO&H modes have the same hardware circuitry. The only difference being the programmed HOLD time. The open and close (negative and positive) selection of the VGS mode is done by controlling the U/D line of the 5 bit counter through the multiplexer U21.



WALK: Integrators RC time set so that the Ramp reachs +6.4v in 25.5 secs. Walk time is set using 8 bit DAC

HOLD: N = ½ (HOLD TIME) Msec - 4 Msecs

DWELL: N = ½ (DWELL TIME) Msec

FIGURE 3.3.4.c: Timing Diagram of VGS & HOH Waveform

3.3.5 PARABOLIC RAMP FUNCTION FOR VGS MODE

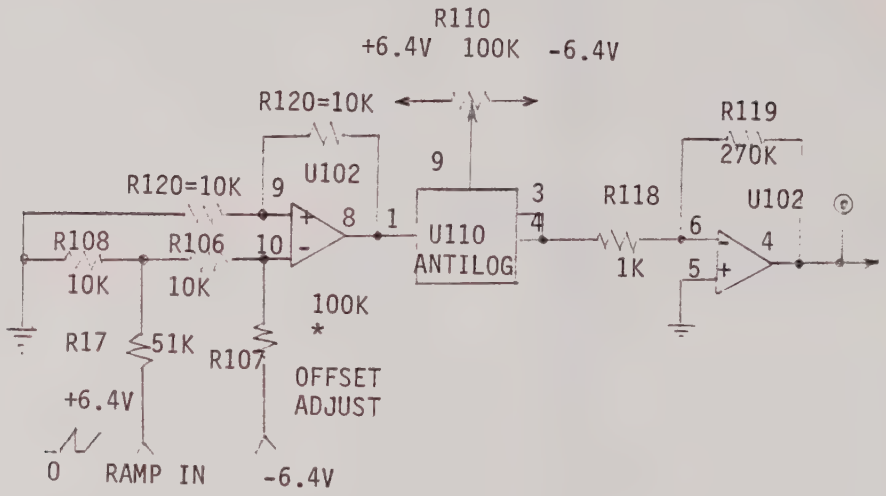


Figure 3.3.5.a: Parabolic Ramp Circuit Diagram

The circuit to generate the parabolic waveform is shown in Figure 3.3.5a. The linear ramp waveform of Figure 3.3.4a is fed into a voltage scaler network U102 and the antilog amplifier U100. The voltage scaler network provides a negative ramp at the anti log-amp input which in turn produces the parabolic waveform at the output. It is then amplified to generate 0-6.4V parabolic waveform at TP108 which has the same amplitude as the linear input waveform at TP107 (see Figure 3.3.5b).

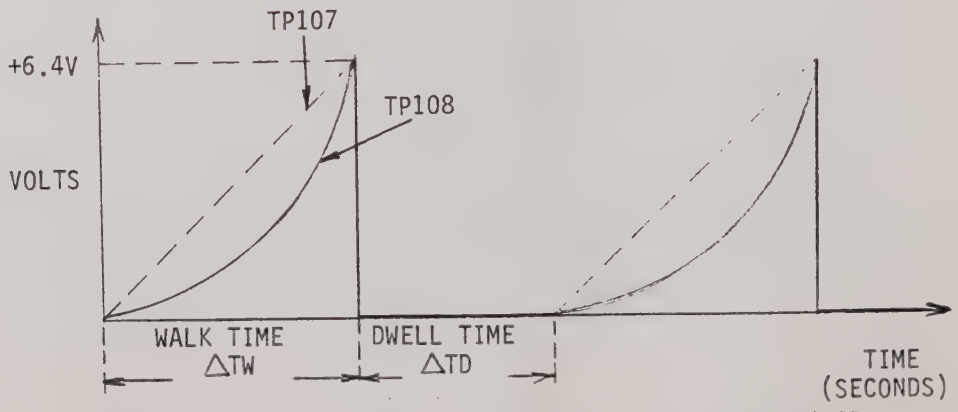


FIGURE 3.3.5.b: Parabolic vs. Linear Ramp Waveforms

3.3.6 RANDOM VOLTAGE SEQUENCER FOR RD

Random numbers from a table stored in the PROM are sent to the SAM OFFSET DAC U104. Each random number gives a random voltage the maximum being 6.4V at TP117. This voltage is further attenuated to the required maximum deviation through U110. This voltage is held for a preprogrammed amount of time anywhere from 200 μ s to 20 ms and further attenuated through the attenuation DAC U101, the scaler U102 and then fed to the Voltage/Frequency converter U108 which gives random frequencies and hence random maximum deviations of the carrier. (See Figure 3.3.6).

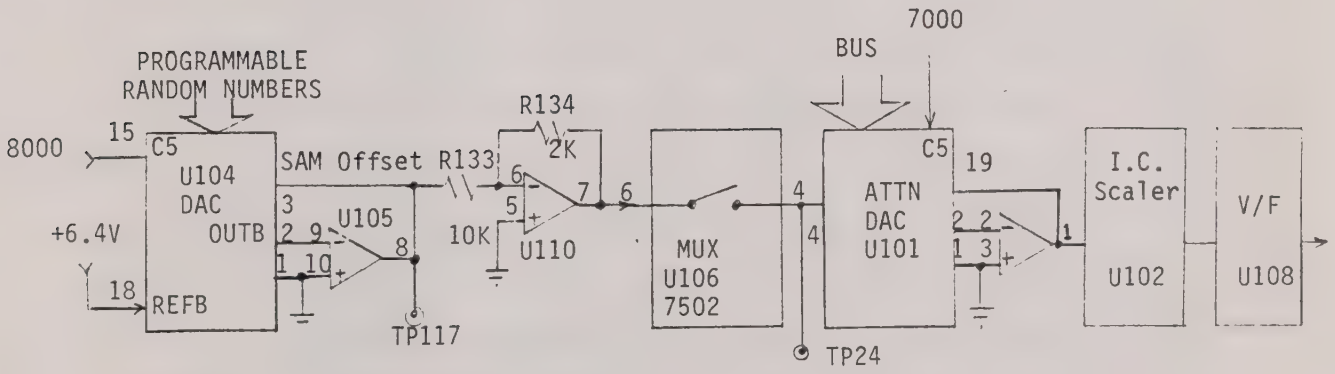


Figure 3.3.6: RD Circuit Diagram

3.3.7 VARIABLE GAIN AMPLIFIER FOR VGS, HOH, RD, VGS & RSAM MODES

The linear, parabolic, RD or External voltage function at TP124 now enters the reference input of a Digital to Analog converter U101. (See Figure 3.3.7.a). The DAC is hooked up so that it behaves as a variable gain amplifier. It allows the high limit of the frequency translation to be adjustable by digital code (i.e. 6.4v value is adjustable) entered via software. Figure 3.3.7b shows the linear ramp function as it corresponds to frequency versus time.

The maximum settable voltage (V_1) will correspond to a 127.5 KHz translation frequency and the minimum voltage V_n will correspond to a 500 Hz translation frequency.

3.3.8 VOLTAGE TO FREQUENCY CONVERTER U108

The Linear, Parabolic, Random or External Voltage function which now has been set for a specific stop translation frequency is used to drive a voltage frequency converter U108 (VFC). The VFC is a free running (astable) voltage controlled multivibrator (see Figure 3.3.8). The effective currents from the four inputs (A,B,C, and D) are summed at the minus input of operational amplifier A_1. A_1 and transistor Q_1 from a preicsion current pump, producing current I, from the collector of Q_1, which is a linear function of the A_1 input currents. Current I, charges capacitor C at a rate which is a precise linear function of the V to F input.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a constant

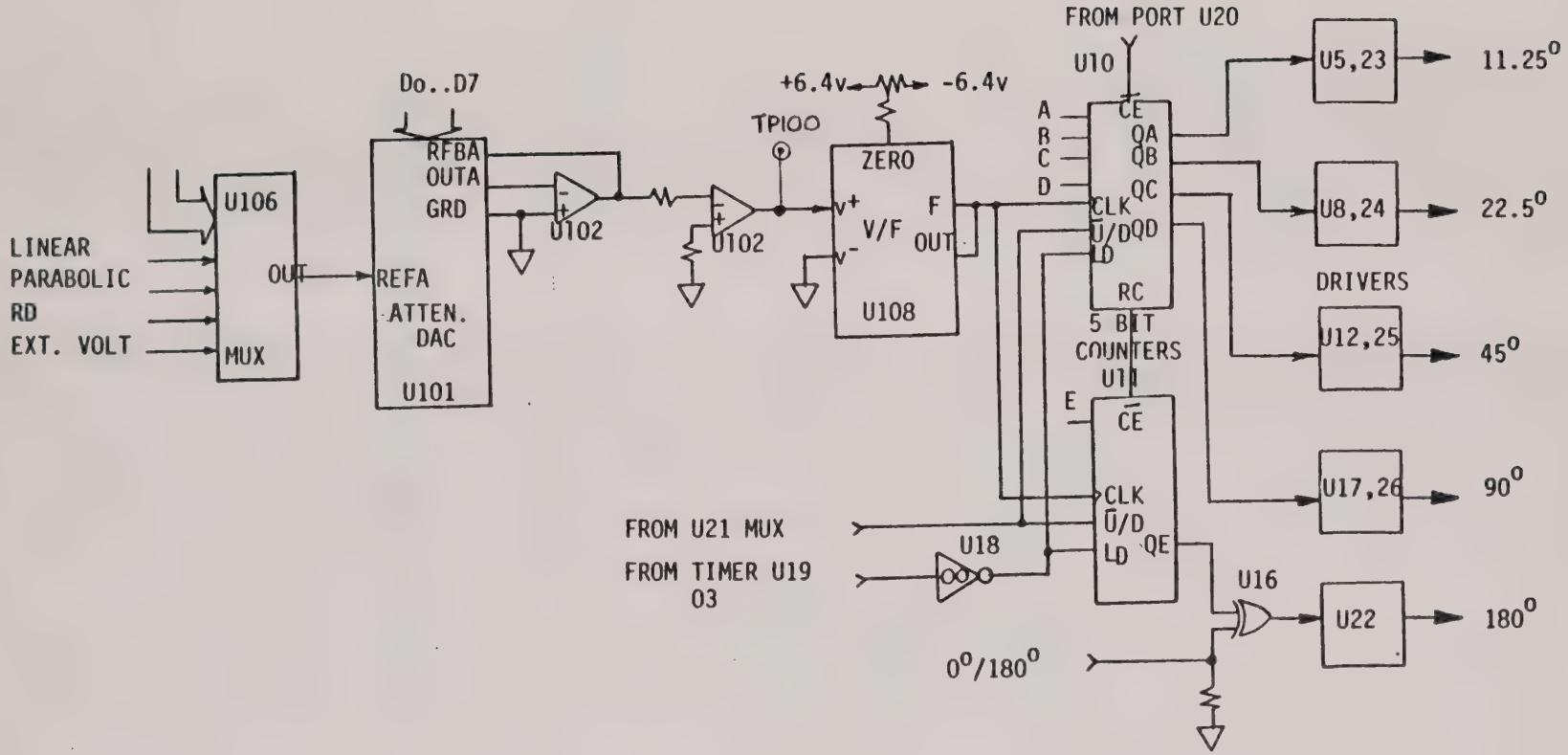


FIGURE 3.3.7.a BLOCK DIAGRAM OF THE ATTENUATION, V/F, COUNTERS & DRIVERS CIRCUITRY

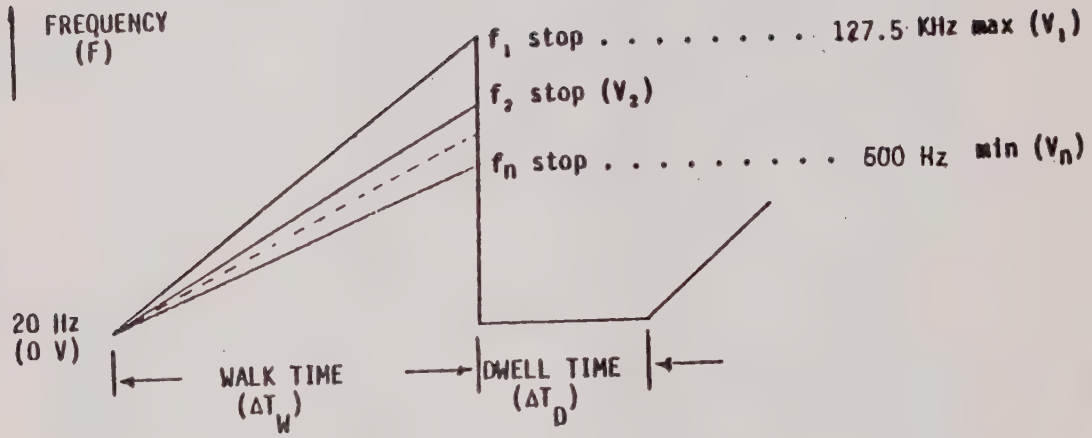


FIGURE 3.3.7.b

LINEAR RAMP FUNCTION SHOWING STOP TRANSLATION FREQUENCY VERSUS TIME

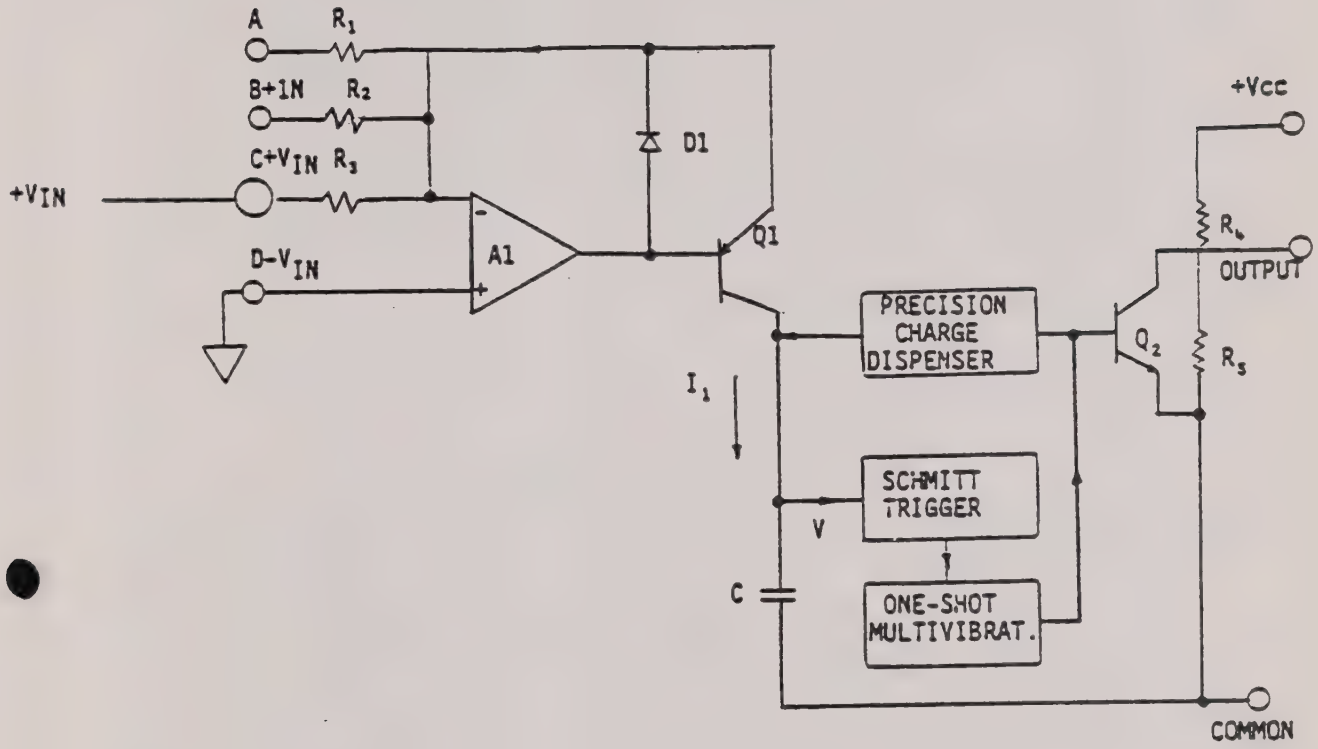


FIGURE 3.3.8

BLOCK DIAGRAM OF VOLTAGE-TO-FREQUENCY CONVERTER

width output pulse. This pulse performs two functions. Amplified by Q_2 which is the output of the V to F and it also functionally activates the Precision Charge Dispense (PCD). The PCD discharges C to the same reference level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the input signal. That is, the rate of charging C, (the repetition rate of charging C and thus the output frequency) is a function of the V to F voltage and/or current inputs.

3.3.9 FREQUENCY TRANSLATION DRIVER

The voltage function at TP100 is given a fixed gain to properly calibrate the frequency translation.

The voltage function which now has been set for a specific stop translation frequency is now used to drive a voltage to frequency converter U108 (VFC). The zero offset trimmer R114 is adjusted to obtain the first start frequency. The TTL output pulse of the VFC which in turn become the clock of the 5 bit up/down counters U10, U11. The U/D line of the counter is controlled by a dual channel multiplexer U21. The load input of the counters U10, U11 is connected to the dwell line which runs low showing the dwell period, thus preventing the counters from counting. Also the chip enable line of the counter U10 is connected to the port Q3 through U20 and is controlled through software. The output of the counters is then fed into the pin diode drivers U5, U8, U12, U17, U22 through U26 to provide proper current, switching speed to drive the phase shifter. Except for the 180° phase cell, the 11.25°, 22.5°, 45°, 90° cells are driven by a pair of complementary type of logic input for better isolation purposes.

In order to illustrate the manner in which the phase shifter is driven by the 5-bit digital code and how the frequency is translated linearly as a function of time, a numerical example of VGS will be used. Consider a walk time of 1 second, a dwell time of 0.5 sec and a stop frequency of 50 KHz.

Figure 3.3.9a shows the relationship between the walk time and the digital drive to the phase shifter. The slope of the walk time ramp 50KHz. The time interval $t_1 = \frac{1}{f_o(32)} + 5\ \mu$ sec where 5 μ sec is the set-up time of the VFC. Hence t_1 = 1.567 msec. Using the relationship:

$$\frac{f_1 - 20}{1.567\ \mu \text{ sec}} = 50\text{KHz we get } f_1 = 98.375\ \mu \text{ sec}$$

Similarly, any given frequency point can be computed using the general equation:

$$\frac{f_n - f_{n-1}}{t_n} = \frac{\Delta F}{\Delta T_w}$$

Since the rate at which the binary counters are clocked is changed linearly, the drive to the phase shifter as shown in Figure 3.3.9.b will be of a second order curve type. The critical break point will occur when the duration t_n is less than 5 μ sec where more than one clock cycle may drive the phase shifter at the same frequency. This would still imply a linear frequency translation with the frequency occurring at some point for more than one clock cycle of the counter. In this manner, the entire translation takes place with each second order dirve curve possessing 32 steps. Each step will be an increasing function of frequency. When the counter is clocked at a rate of 32 x (50 KHz) the entire process will stop for the duration of the

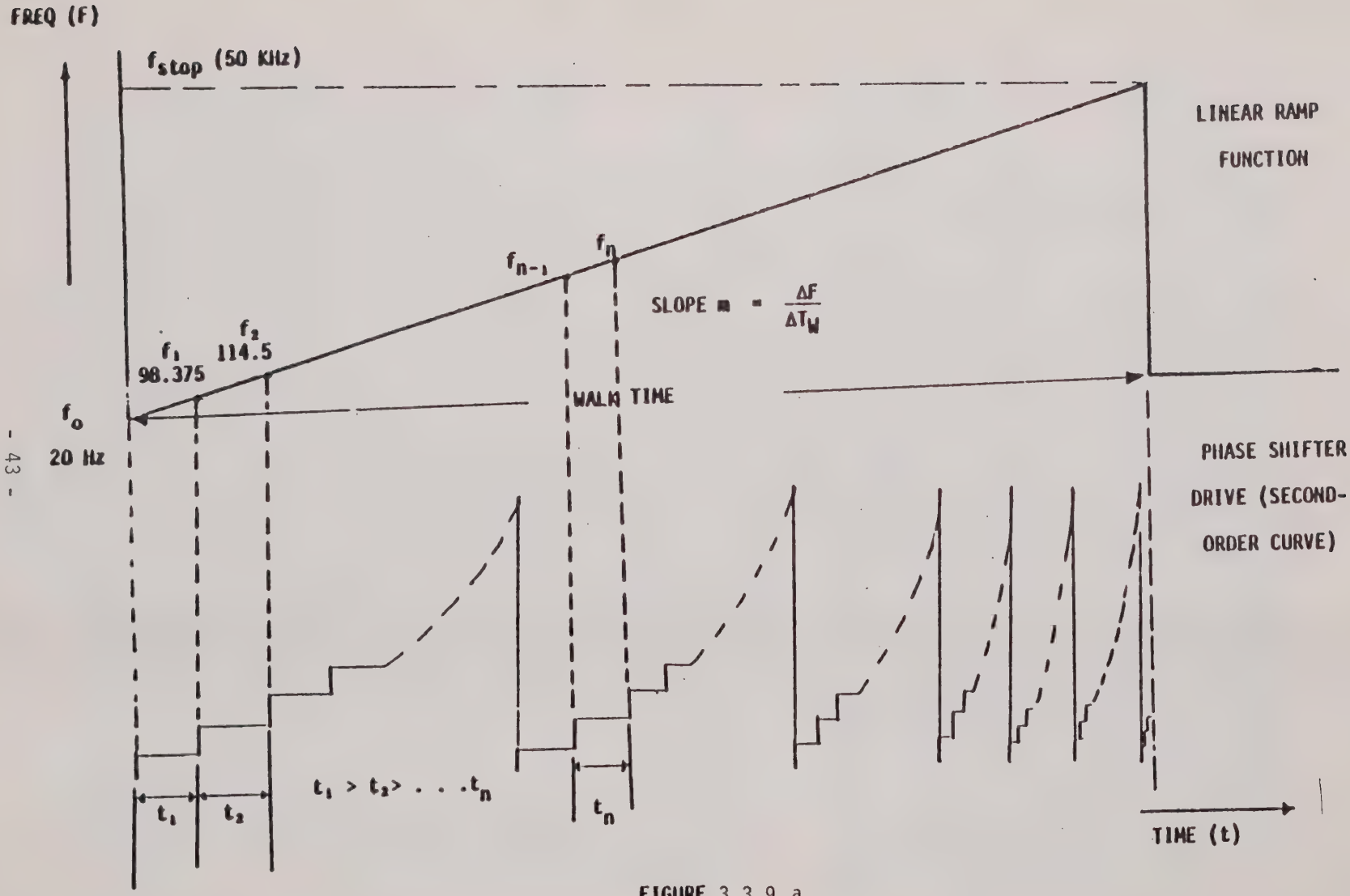


FIGURE 3.3.9.a

PHASE SHIFTER DRIVE FOR LINEAR FREQUENCY TRANSLATION

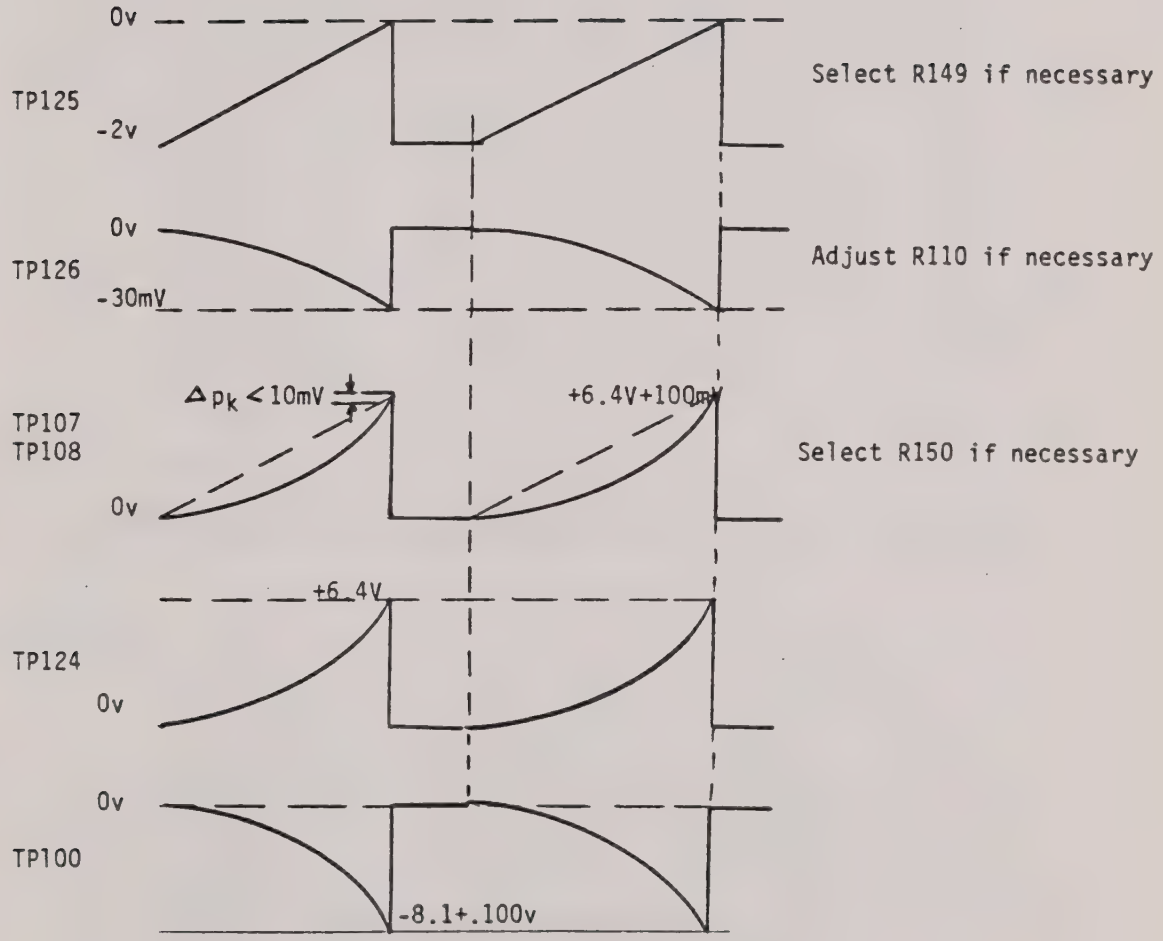


FIGURE 3.3.9.b:TIMING DIAGRAM FOR PARABOLIC WAVEFORMS.

dwell time (with the phase shifter not performing any translation) before starting again.

The function generator also provides translation of the frequency in the second order type. Figure 3.3.9.b shows the actual parabolic waveform at TP108 generates from the linear waveform at TP107. The logarithm amplifier U100 is used as the anti-log module to generate this parabolic function, the operational amplifier U102 is to scale, the waveform at TP108 to be identical to TP107 at both end points. The multiplexer U106 allows the operator to select either the linear or parabolic function. When the parabolic function is selected, the 0 to 6.4v second order curve ($Y=KX^2$) is generated at TP124. This second order curve is then fed to the multiplying DAC U101 and the operational amplifier U102 to attenuate the waveform at TP100.

3.3.10 SWEEP VOLTAGE GENERATOR FOR NARROW BAND REPEATER NOISE (NBRN)

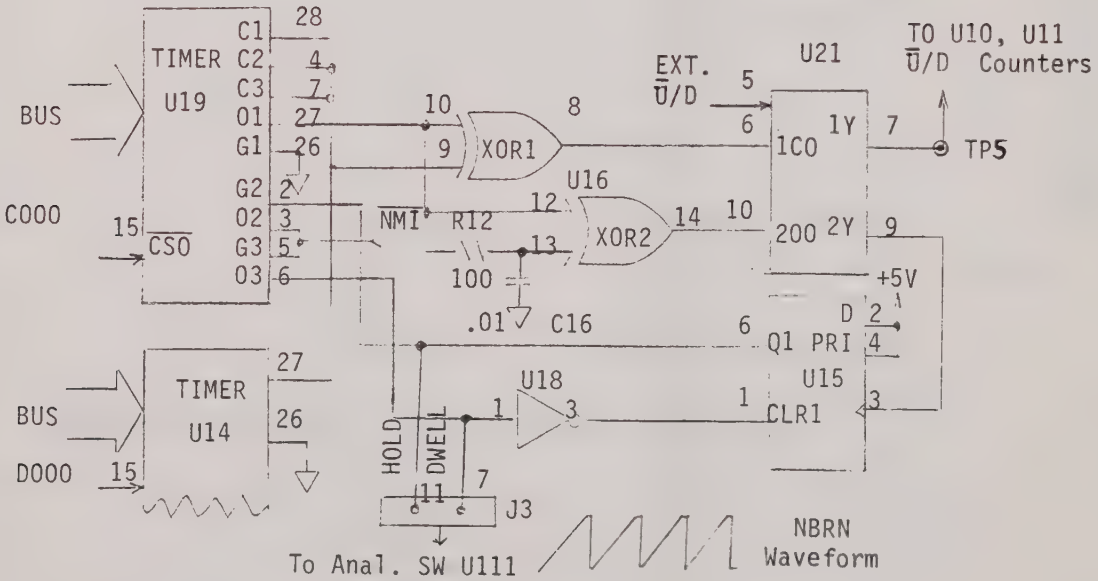


Figure 3.3.10.a: NBRN Circuit Diagram and Waveform

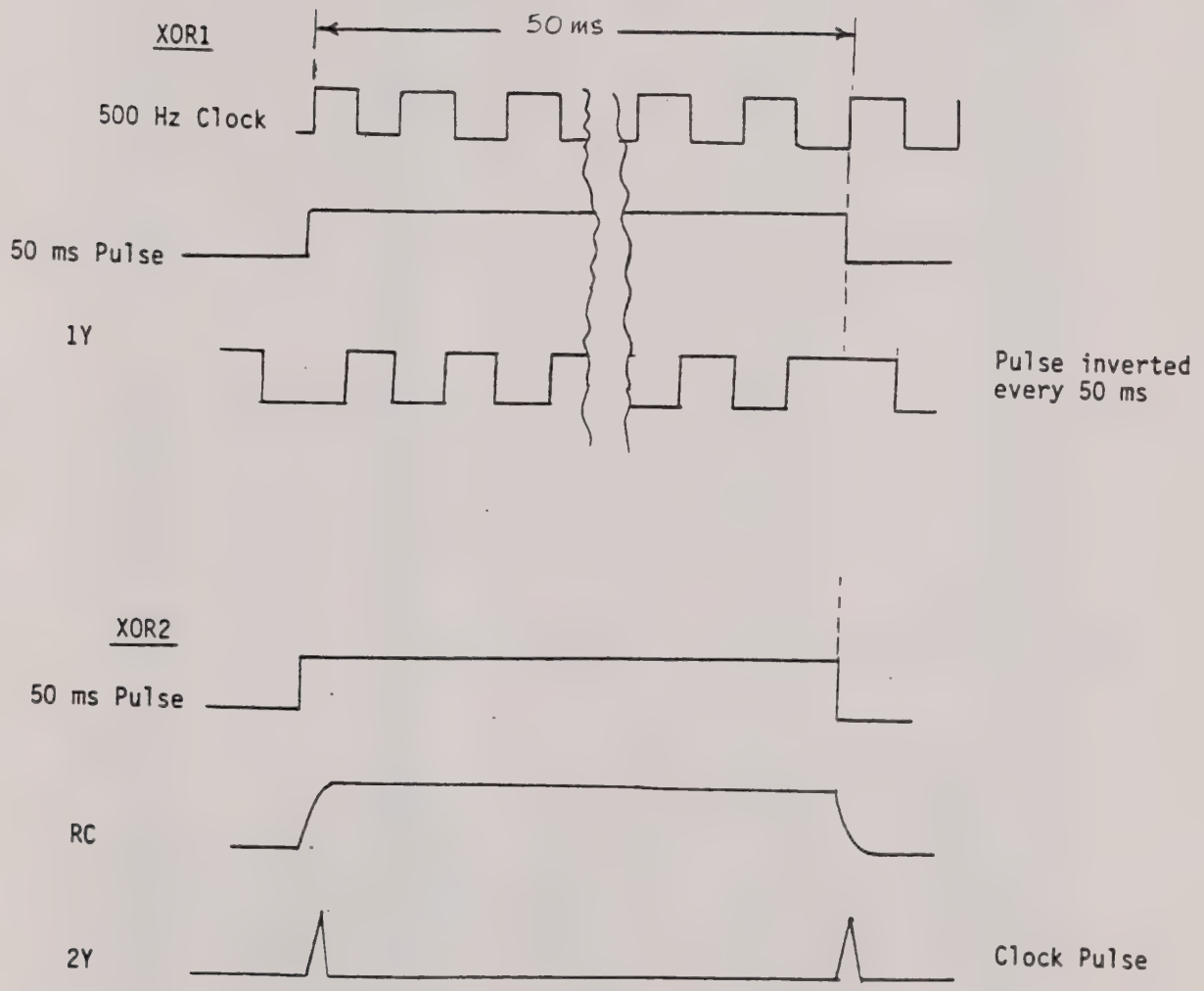


FIGURE 3.3.10.b: Timing Diagram for NBRN

The circuitry to generate the swept voltage generator for NBRN is shown in Figure 3.3.10a. Timer U14 generates an output pulse of 500 Hz frequency. This pulse clocks the three internal timers 01, 02 and 03 in U19. As the NBRN mode is initiated, Timer 01 of U19 starts counting. At the end of 50 ms the RC network with the XOR2 gate gives a 1 msec pulse which through the multiplexer U21 clocks the flip flop U15. Q1 goes low and triggers the whole process of HOH and DWELL. Keeping the hold and dwell time periods very small gives us the required waveform. This process is explained in detail under hold and dwell circut on Section 3.3.4.

Output from 1Y at U21 flips state every millisecond due to the nature of the pulse. The 50 ms pulse from Timer 01 of U19 inverts the pulse train at the end of 50 ms. Timing diagrams are shown in Figure 3.3.10b.

3.3.11 RANDOM VOLTAGE GENERATOR FOR PRN & BPRN

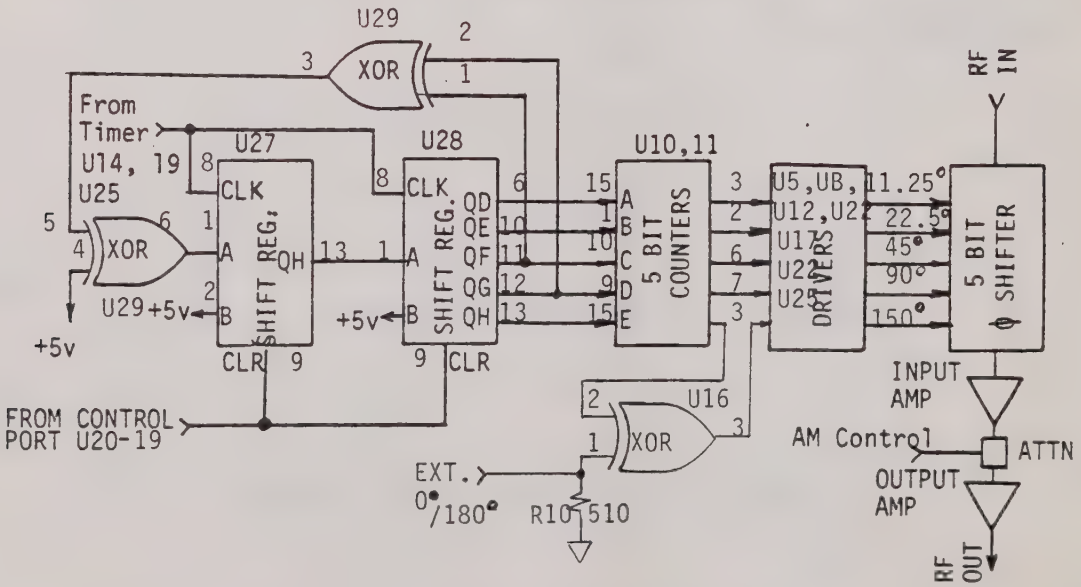


Figure 3.3.11: PRN & BPRN Circuit Diagram

Table 3.3.11: RD Time vs. PRN BW

RANDOM TIME (MSEC)	PRN B.W. (KHZ)	RANDOM TIME (MSEC)	PRN B.W. (KHZ)
.2	5.0000	5.1	.1961
.3	3.3333	5.2	.1923
.4	2.5000	5.3	.1887
.5	2.0000	5.4	.1852
.6	1.6667	5.5	.1818
.7	1.4286	5.6	.1786
.8	1.2500	5.7	.1754
.9	1.1111	5.8	.1724
1.0	1.0000	5.9	.1695
1.1	.9091	6.0	.1667
1.2	.8333	6.1	.1639
1.3	.7692	6.2	.1613
1.4	.7143	6.3	.1587
1.5	.6667	6.4	.1563
1.6	.6250	6.5	.1538
1.7	.5882	6.6	.1515
1.8	.5556	6.7	.1493
1.9	.5263	6.8	.1471
2.0	.5000	6.9	.1449
2.1	.4762	7.0	.1429
2.2	.4545	7.1	.1408
2.3	.4348	7.2	.1389
2.4	.4167	7.3	.1370
2.5	.4000	7.4	.1351
2.6	.3846	7.5	.1333
2.7	.3704	7.6	.1316
2.8	.3571	7.7	.1299
2.9	.3448	7.8	.1282
3.0	.3333	7.9	.1266
3.1	.3226	8.0	.1250
3.2	.3125	8.1	.1235
3.3	.3030	8.2	.1220
3.4	.2941	8.3	.1205
3.5	.2857	8.4	.1190
3.6	.2778	8.5	.1176
3.7	.2703	8.6	.1163
3.8	.2632	8.7	.1149
3.9	.2564	8.8	.1136
4.0	.2500	8.9	.1124
4.1	.2439	9.0	.1111
4.2	.2381	9.1	.1099
4.3	.2326	9.2	.1087
4.4	.2273	9.3	.1075
4.5	.2222	9.4	.1064
4.6	.2174	9.5	.1053
4.7	.2128	9.6	.1042
4.8	.2083	9.7	.1031
4.9	.2041	9.8	.1020
5.0	.2000	9.9	.1010
		10.0	.1000

Table 3.3.11 (cont'd.)

RANDOM TIME (MSEC)	PRN B.W. (KHZ)	RANDOM TIME (MSEC)	PRN B.W. (KHZ)
10.1	.0990	15.1	.0662
10.2	.0980	15.2	.0658
10.3	.0971	15.3	.0654
10.4	.0962	15.4	.0649
10.5	.0952	15.5	.0645
10.6	.0943	15.6	.0641
10.7	.0935	15.7	.0637
10.8	.0926	15.8	.0633
10.9	.0917	15.9	.0629
11.0	.0909	16.0	.0625
11.1	.0901	16.1	.0621
11.2	.0893	16.2	.0617
11.3	.0885	16.3	.0613
11.4	.0877	16.4	.0610
11.5	.0870	16.5	.0606
11.6	.0862	16.6	.0602
11.7	.0855	16.7	.0599
11.8	.0847	16.8	.0595
11.9	.0840	16.9	.0592
12.0	.0833	17.0	.0588
12.1	.0826	17.1	.0585
12.2	.0820	17.2	.0581
12.3	.0813	17.3	.0578
12.4	.0806	17.4	.0575
12.5	.0800	17.5	.0571
12.6	.0794	17.6	.0568
12.7	.0787	17.7	.0565
12.8	.0781	17.8	.0562
12.9	.0775	17.9	.0559
13.0	.0769	18.0	.0556
13.1	.0763	18.1	.0552
13.2	.0758	18.2	.0549
13.3	.0752	18.3	.0546
13.4	.0746	18.4	.0543
13.5	.0741	18.5	.0541
13.6	.0735	18.6	.0538
13.7	.0730	18.7	.0535
13.8	.0725	18.8	.0532
13.9	.0719	18.9	.0529
14.0	.0714	19.0	.0526
14.1	.0709	19.1	.0524
14.2	.0704	19.2	.0521
14.3	.0699	19.3	.0518
14.4	.0694	19.4	.0515
14.5	.0690	19.5	.0513
14.6	.0685	19.6	.0510
14.7	.0680	19.7	.0508
14.8	.0676	19.8	.0505
14.9	.0671	19.9	.0503
15.0	.0667	20.0	.0500

The five bit parallel-out serial shift registers U27 and U28 is implemented together with the Exclusive-OR gate U29 to generate the pseudo random noise (PRN) mode of the deception module (see Figure 3.3.11). A pair of Exclusive-OR gates form a feedback function in the circuit. Serial data is being fed into the A input of U27 and shifted out to the other A input of U28 in which the shift clock is controllable by the timer. The random digital codes are generated by shifting out data circularly. These random codes are then fed to the 5 bit counter, driver and directly to the phase shifter for serrodyning. The clock rate of shifting is programmable through RD mode to determine the bandwidth of the PRN mode The CLR control port is to activate the PRN mode. The blinking PRN is generated as the same manner as the PRN (BPRN) mode except the AM is being applied to the pin attenuator. The fixed frequency AM of BPRN mode is programmable from 0.1 HZ to 25.5 Hz in 0.1 Hz steps which is 1/100 of the frequency set in the MFR mode. The duty cycle is identical to the MFR duy cycle set in the MFR MODE.

3.3.12 SWEPT VOLTAGE GENERATOR FOR RSAM AND VGS&RSAM

3.3.12.1 SWEPT VOLTAGE GENERATOR FOR RSAM

The RSAM circuit diagram is shown in Figure 3.3.12.1a. An integrator circuit combined with a digital-to-analog (DAC) is used to generate a ramp voltage (0-6.4V). The operation of the integrator and DAC is essentially the same as that discussed in "Section 3.3.4". Except that there is no provision for hold and dwell time. The ramp is reset using an RC circuit. In the RSAM

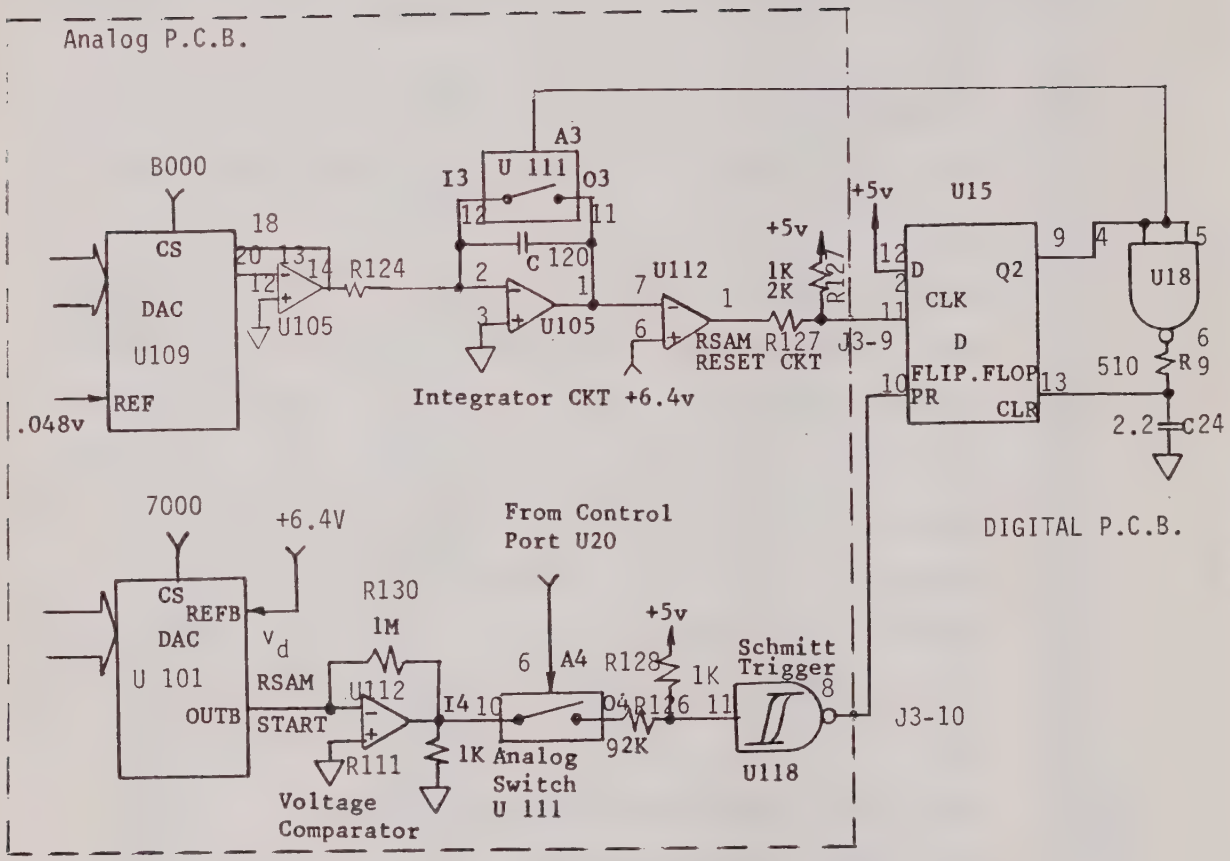


Figure 3.3.12.1.a: VGS & RSAM Circuit Diagram

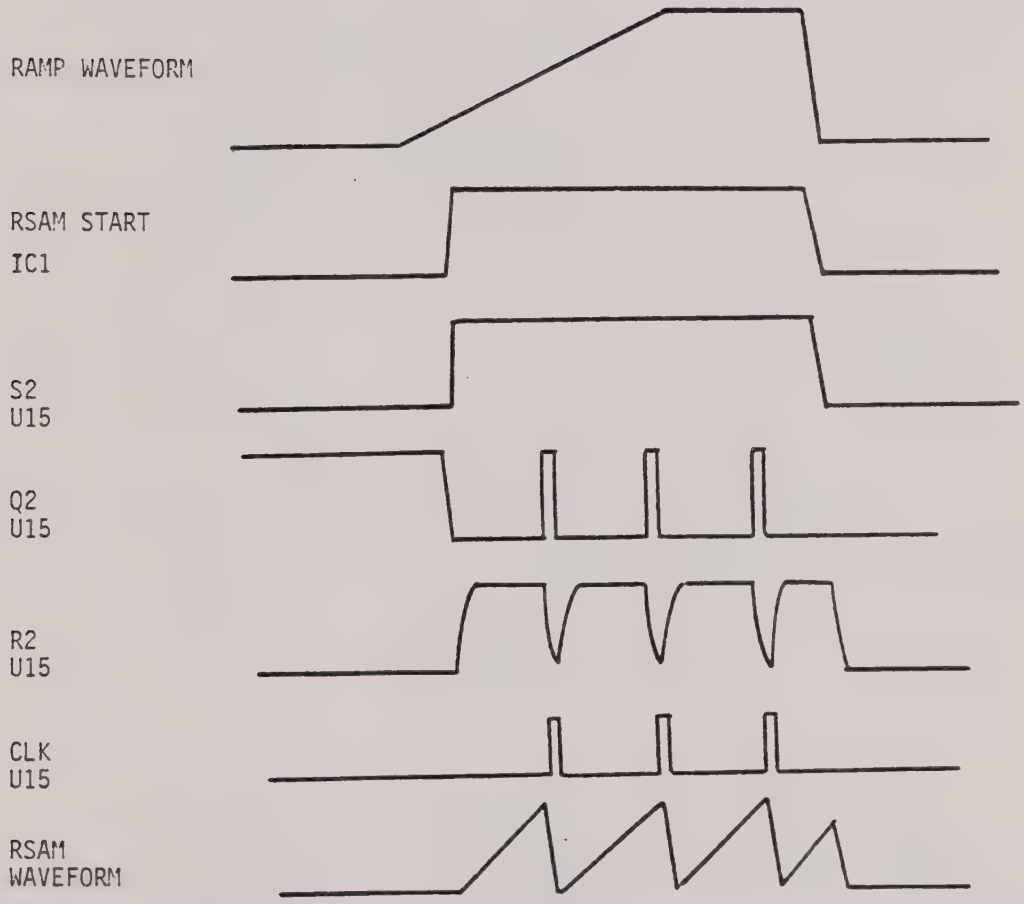


FIGURE 3.3.12.1.b: THE TIMING DIAGRAM OF RSAM CIRCUITRY

mode, the RSAM start is disconnected from the preset input using the analog switch U111 which is software controlled through the port device.

Q2 output is low and U111 open, the ramp voltage at the integrator starts to ramp up to 6.4V, then the comparator U112 triggers a one shot pulse to the clock input of the D Flip Flop U15. This clocks a high pulse at output Q2 and close U111 to discharge the RC circuit of the integrator. Meanwhile, a low at clear input of U15 resets the flip-flop after a small predetermined delay. After flip-flop being reset, U111 open and the RSAM integrator start, repeat the ramp up cycle until the dwell time of the walk DAC operates. The timing diagram of the RSAM circuit is shown in Figure 3.3.12.1.b.

3.3.12.2 RSAM ATTENUATION AND OFFSET

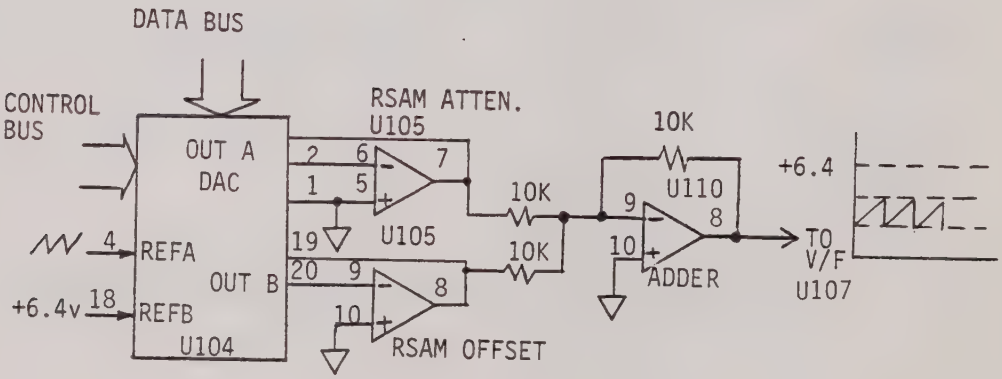


Figure 3.3.12.2: Circuitry for RSAM Attenuation and Offset

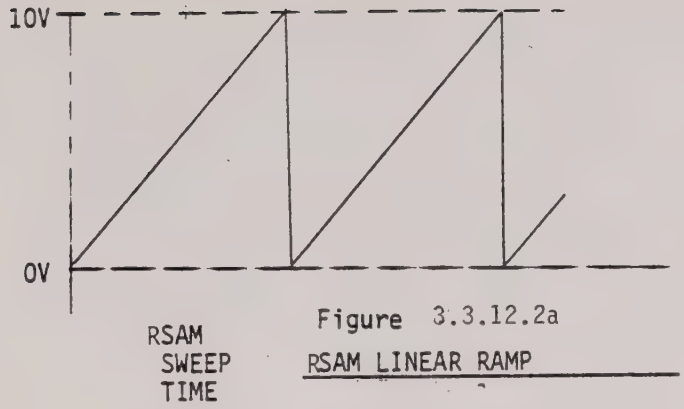


Figure 3.3.12.2a
RSAM LINEAR RAMP

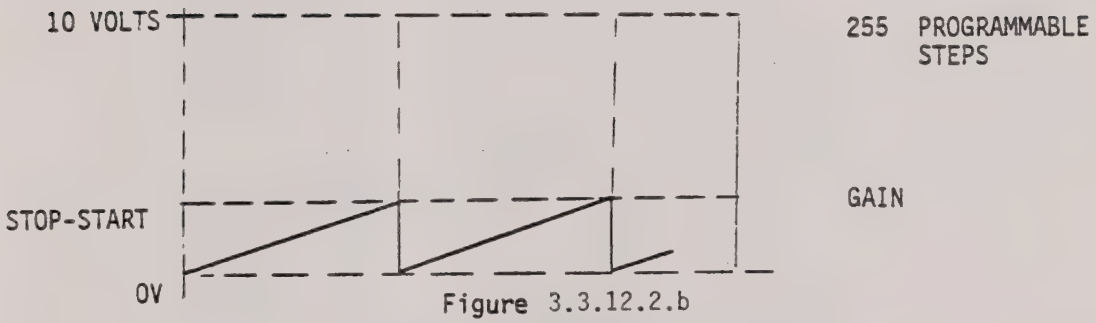


Figure 3.3.12.2.b
RSAM LINEAR RAMP WITH GAIN

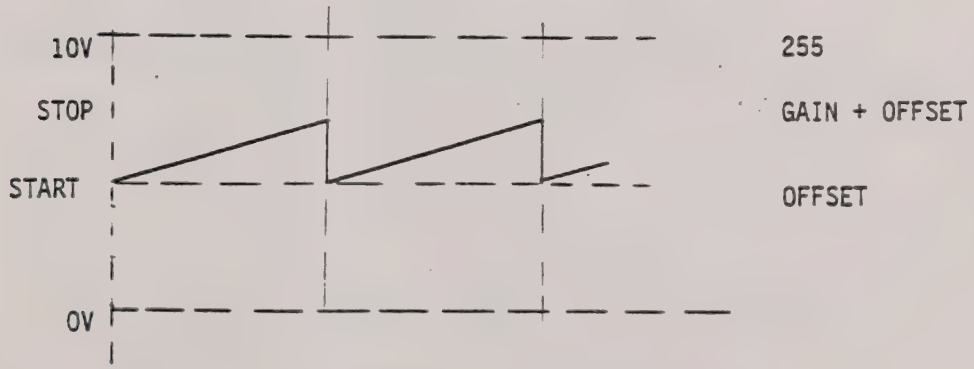


Figure 3.3.12.2.c
RSAM LINEAR RAMP WITH GAIN AND OFFSET

The RSAM ramp which has already been set for a fixed sweep time now passes through a DAC U104 hook up such that the A channel is a programmable voltage gain amplifier and the B channel is a programmable offset control. (See Figure 3.3.12.2). The slope of the RSAM signal can be varied as shown in the Figure 3.3.12.2.a,b,c This attenuated signal is added to a programmable offset to produce the ramp as shown.

3.3.12.3 RSAM V/F & Duty Cycle

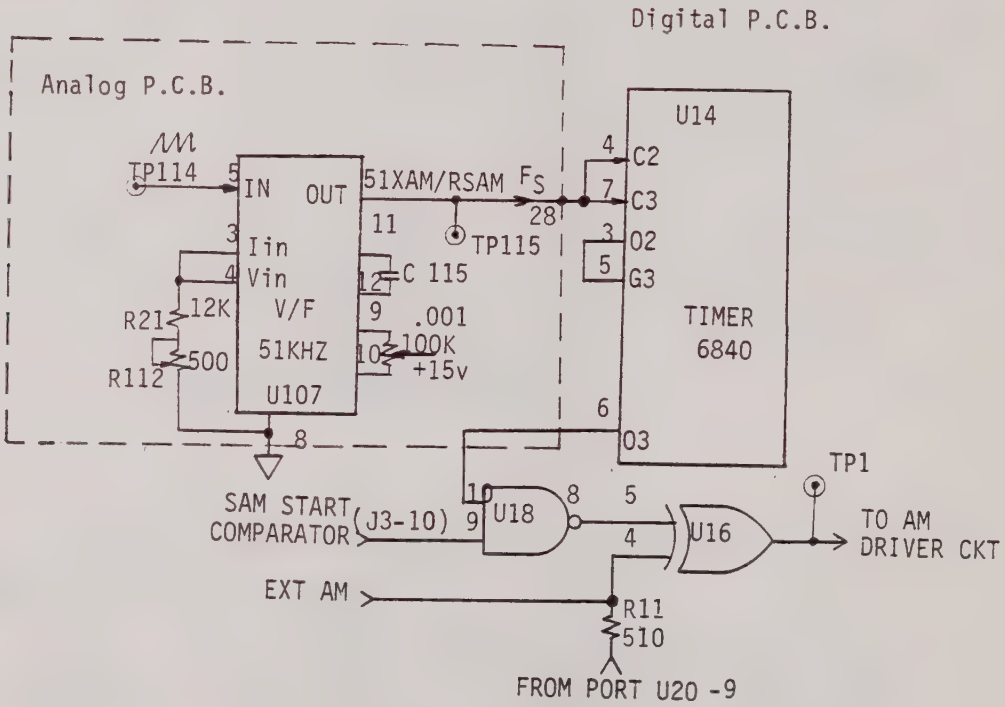


FIGURE 3.3.12.3.a CIRCUITRY FOR RSAM V/F & DUTY CYCLE

The swept voltage now passes through a linear VFC U107. The VFC is set for 51.0 KHz at 6.4V. The swept voltage limit controls the

frequency of amplitude modulation. The VFC output clocks two timers at U14 (see Figure 3.3.12.3.a) The timers have been programmed to give the frequency limit specified for each mode. In the RSAM mode, the frequency limit specified was 1275 Hz. Hence, to scale 51.0 KHz down to 1275 Hz, a divide by 40 pulse is programmed in Timer O_2.

i.e. $$\frac{51.0}{40} \text{ KHz} = 1275 \text{ Hz}$$

To obtain the duty cycle, the input value of duty cycle was scaled down to within 40 using the equation.

Programmed duty cycle pulse for Timer O_3 = $\frac{\text{Input value of duty cycle}}{2.5}$

The timing diagrams are shown in Figure 5.3.12.3. b.

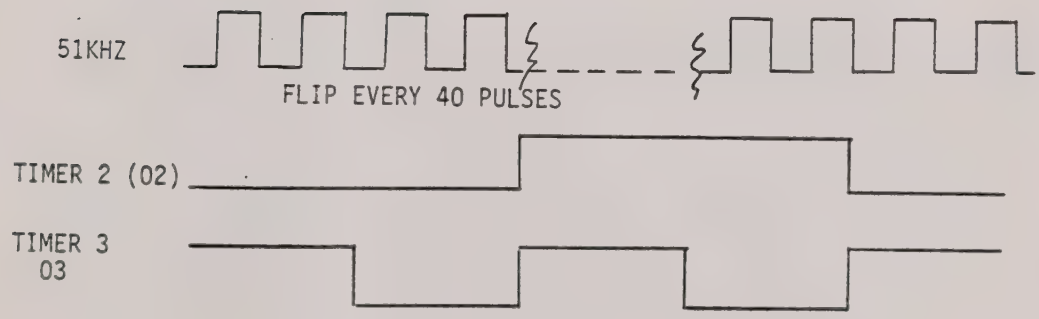


Figure 3.3.12.3 b: Timing Diagram for RSAM & Duty Cycle

The AM signal from Timer O_3 goes out of the NAND gate only when the signal from the SAM START Comparator goes high. The output from the NAND gate is again gated by an exclusive OR U16. One of the inputs of the XOR is for external control of AM, the same input is also software controllable by the port U20 pin 9.

3.3.12.4 TRANSLATION FREQUENCY DETECTOR FOR RSAM START

When operating the VGS & RSAM, RSAM must be triggered by a programmable translation frequency (see Figure 3.13.12.1.a). This is accomplished by detecting the voltage Vd which corresponds to that frequency at the input of the VFC U108 for frequency translation. The programmable detector consists of a digital to analog converter and a comparator U112. The D/A U101 is programmed with the voltage corresponding to the desired translation frequency. When the translation voltage passes the programmed D/A voltage, the comparator flips starting a new RSAM sweep while the VGS is still running. The Schmitt trigger U118 is used to improve the transition time.

3.3.13 SINGLE VOLTAGE GENERATOR FOR MFR AND CDB AND STBY

Fixed number is sent to the SAM OFFSET DAC U104 where output at TP114 is a fixed voltage (see Figure 3.3.12.2). This gives a fixed frequency from the output of the voltage to frequency converter U107. This frequency is then fed into the timer U14 through J3-28 to scale 51 KHz down to 2550 Hz, a divide by 20 pulse is programmed in the Timer 02.

$$\text{i.e} \qquad \frac{51.0 \text{ KHz}}{20} = 2550 \text{ Hz}$$

The programmed duty cycle pulse for

$$\text{Timer } O_3 = \frac{\text{Input value of duty cycle.}}{2.5}$$

The actual MFR signal output O3 at U14-6 is then fed into gates U18, U16 and to TP1 through J3-12 and J3-36. The NPN transistor Q1 serves as the TTL driver to attenuate the VDA power output to the selected MFR parameters.

For the CDB mode, the timer U114 is utilized to obtain 1/100 of MFR frequency.

3.3.14 Circuit Description for STBY and REPEATER Mode

The VDA STBY and REPEATER Mode is generated by keeping the low logic at U114-6, U15-10 while controlling the TTL Logic at U20-9 port. The signal at U16-6 is then fed into J3-12, J3-36 and to TP1. A high logic at TP1 generates the STBY mode, the NPN transistor driver Q1 is then turned on to drive the attenuator. A low logic at TP1 generates the REPEATER mode.

3.3.15 External Control Signals

The external control signals are generated when the operator selects the external control source at VGS and MFR modes. For the VGS mode, the open/close selection is selected through the multiplexer U21-5. For the MFR mode, the external AM control is selected by setting port U20-9 at TTL low. The external 0°/180° is selected through the input of the EXCLUSIVE-OR gate U16-1. The pull-up resistor 3K should be installed for these external control functions.

3.4 Power Supply Circuit Description

Figure 3.4 shows the detailed schematic of the power supply circuitry. The transient suppressor A105 is to suppress the transient

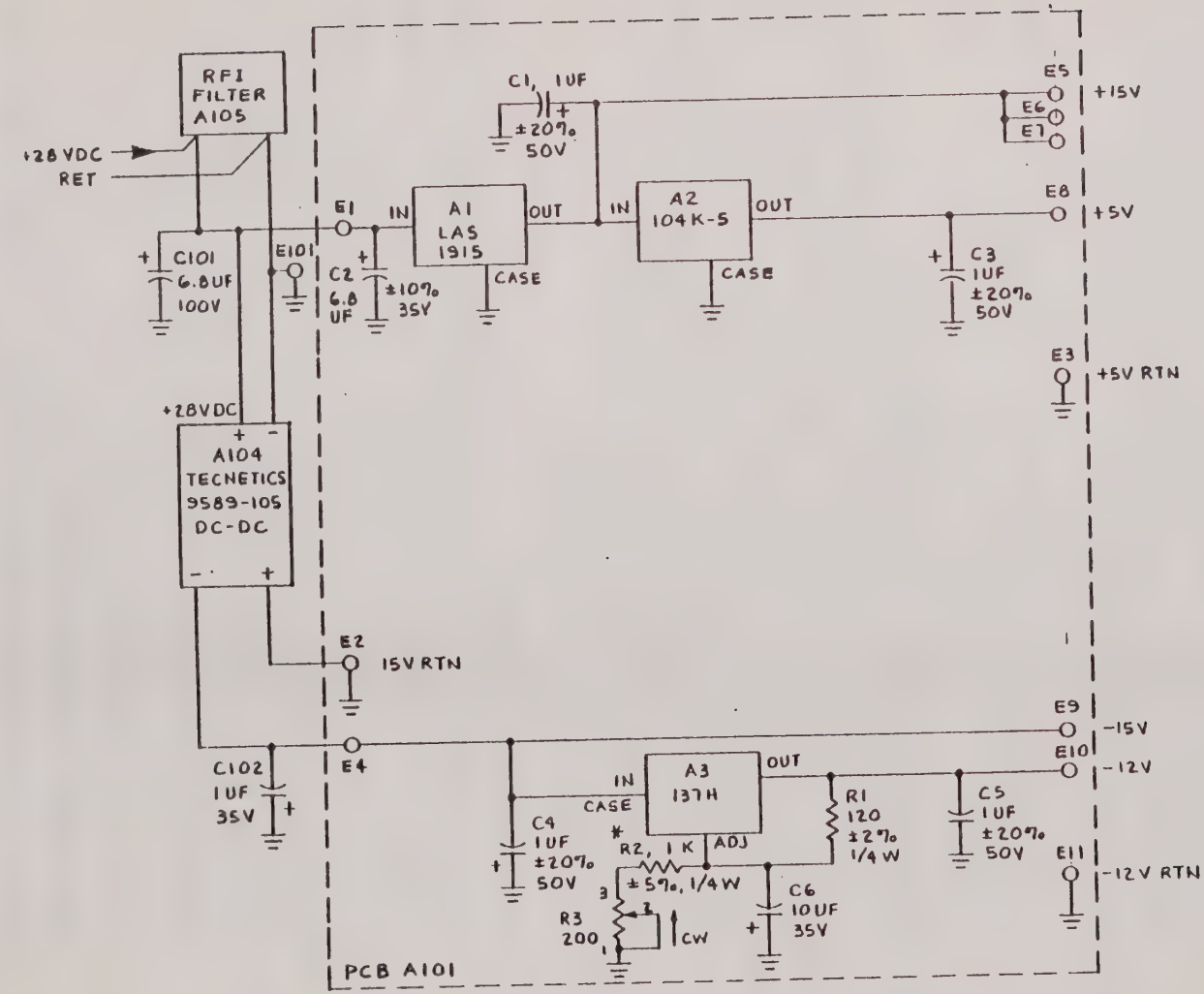


Figure 3.4: VDA Power Supply Circuitry

when tuning the +28V DC power on. the A104 module is to provide -15 VDC to the VDA and DC-DC regulated to -12 VDC through A3 on the A101 PCB. The A1 and A2 TO-3 package to DC-DC regulated the +28 VDC to +15 VDC and +5 VDC. The test points are provided on A101 PCB to check for proper voltages.

3.5 RS-232C INTERFACE CIRCUIT DESCRIPTION

3.5.1 GENERAL DESCRIPTION

Figure 5.18shows the detailed schematic of the RS-232C Interface circuit assembly. Table 3.5 shows the VDA RS-232C Interface specification. The hardware of the RS-232C Interface circuitry comprises of: an asynchronous communications interface adapter U1 (ACIA) to provide the data formating and control to interface serial asynchronous data communications information to bus organized systems from the VDA 6809 microprocessing unit. The U3 and U4 are the line receiver and driver to interface data terminal equipment with data communication equipment. An external control switch at PCB A2 to allow the user to apply external control signals to the VDA once the external control mode was selected.

Table 3.5 RS232C Interface Specification

Transmission Format	:	Asynchronous
Mode	:	Full Duplex
Number of Start Bit	:	1
Number of Data Bits	:	8
Parity	:	0
Number of Stop Bits	:	1
Character Set	:	ASCII
Baud Rate (Selectable)	:	50,75,109,134,150,300,600,1200,1800, 2400,3600,4800,7200,9600,19200
Signal Levesl	:	Mark = -3 to -25 volts Space = +3 to +25 volts
Connector	:	25-pin, Subminiature, D Type, Female
Maximum Cable Length	:	50 feet

TXD (Transmit Data)

This output line is used to transfer serial data from the VDA to the peripheral computer. The least significant bit (LSB) of the transmit data register is the first data bit transmitter and the rate of data transmission is determined by the baud rate selected.

RXD (Receiver Data)

This input line is used to input the serial data into the VDA from the peripheral computer; the least significant bit is the first bit to be received. The receiver data baud rate is the baud rate selected.

DSR (Data Set Ready)

This DSR output line is used to indicate a request to send a signal to the peripheral computer from the VDA. The state level of this line is high.

DATA RTN (Data Return)

The DATA RTN is a common ground between the VDA and the peripheral computer.

3.5.2 OPERATIONS

Transmit character is written into the Transmit Data register. This character is transferred to a shift register where it is serialized and transmitted from the Transmit Data (TXD) output preceded by a start bit and followed by one stop bit. The second character will be automatically transferred into the shift register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

Data is received from a peripheral by means of the Receive Data (RXD) input. In a typical receiving sequence, the status register is read to determine if a character has been received from the peripheral. If the Received Data register is full, character is being transferred to the VDM.

3.6 DATA ENTRY MODULE CIRCUIT DESCRIPTION

The data entry module provides a means for setting parameters by either keypad or remote programming. The data entry module is composed of a 16 character alpha numeric LCD display for prompting and key in verifcation, a calculator style keyboard with 24 keys, a PC Board with a RS232 connector and a interface cable to connect to the VDA (see Figure 3.6.1). The detailed schematic of the data entry module circuit board is shown in Figure 3.6.2. A peripheral interface adapter U1 (PIA) provides a means of interfacing peripheral display to the 6809 microprocessor unit in the VDA. The interface from the MPU to peripherals is through two 8-bit bi-directional peripheral data lenses and four control lines. The PA's port of U1 is configured as the output port and PB's is configured as the input port to activate the

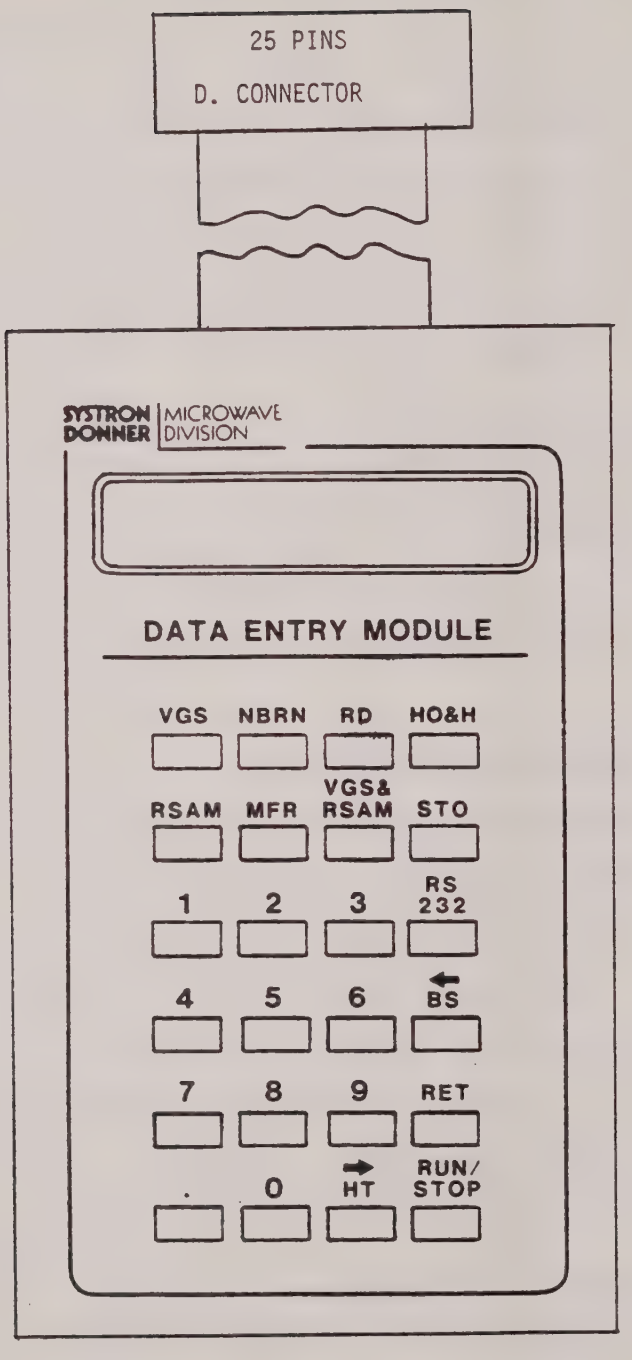
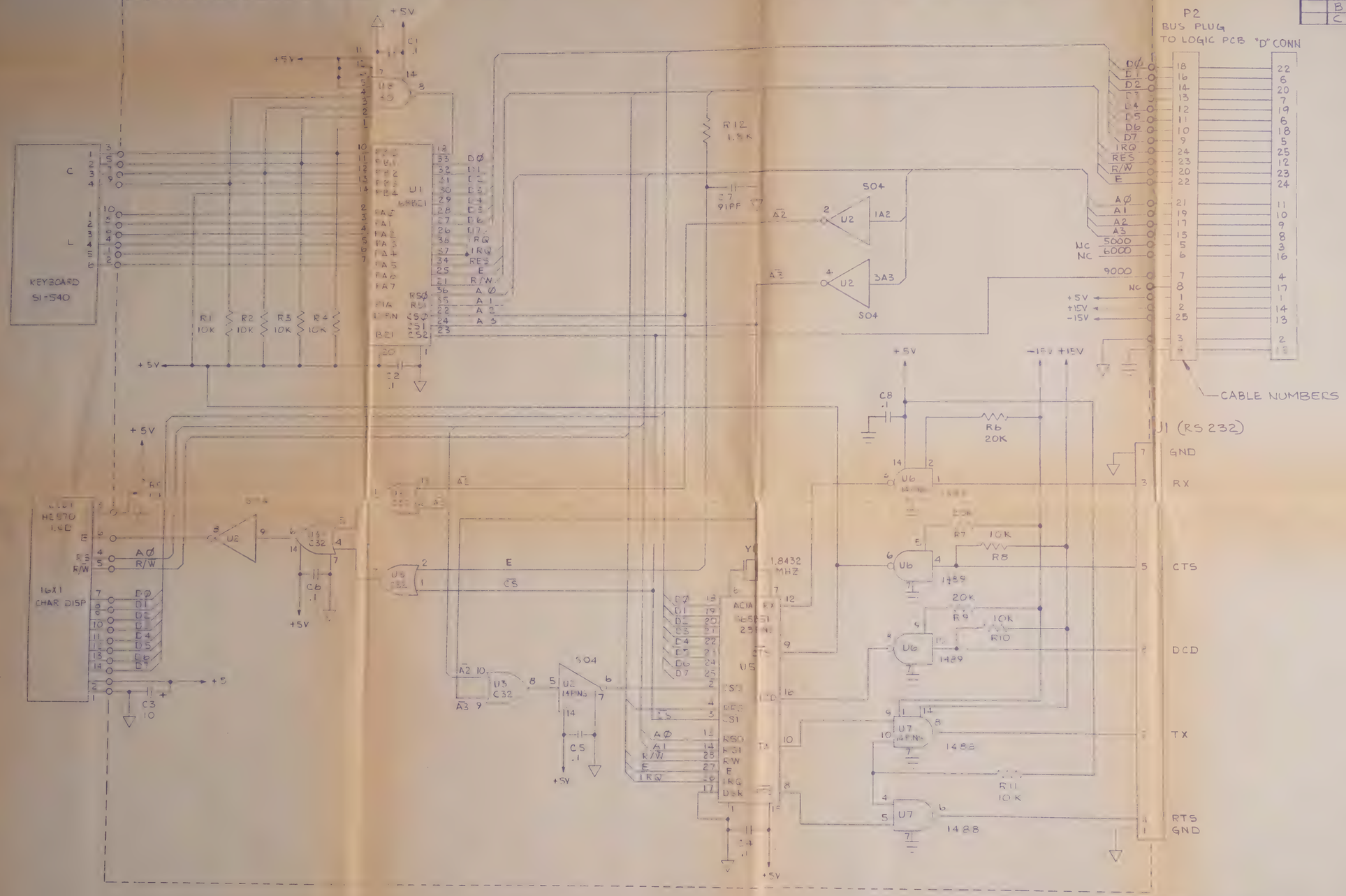


FIGURE 3.6.1: KEYPAD ARRANGEMENT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE PER E.O. 17282	12/30/84	JS
	B	REV. PER EO 18424	10/1/87	JS
	C	REV PER EO 18490	11/30/87	JS



312055	VDM
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND PER ANS Y14.5
FRACTIONS ± | DECIMALS .X ± .02 .XX ± .010 .XXX ± | ANGLES ± ½°
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.
DR BY LAZAR RAJKOVIC 7-2-84
CHK BY
APPROVED BY

SYSTRON DONNER MICROWAVE CORPORATION
4866 OLEARD ST. VAN NUYS, CALIFORNIA 91411

VELOCITY DECEPTION DATA ENTRY MODULE SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.
D	01220	312057

SCALE NONE | SHEET 1 OF 1

keyboard function. The 16x1 character display interfaces directly to the 6809 MPU through the interface cable; the gates U3 and U2 provides proper chip select logic from the VDA to drive the display. An asynchronous communication interface adaptor (ACIA) U5 provides the data formating and control to interface serial asynchronous data communications information to bias organized systems from the VDA 6809 microprocessing unit. The U6 and U7 are the line receiver and driver to interface data terminal unit with data communication unit. Table 3.5 defines the RS-232C interface specifications.

3.6.1 THE RS232C INTERFACE ASSEMBLY

The schematic and interconnect diagram for the RS232C Interface Assembly is shown in Figure 5.18. Table 5.0 described the RS232C specifications. The physical connection to the VDA is shown in the outline drawing OD312068-01, Section 3.0.

Table 3.6a RS232-C Control Information

MODE KEY	CONTROL CHARACTERS	ASCII CODE
VGS	G	47
NBRN	H	48
RD	I	49
HO&H	J	4A
RSAM	K	4B
MFR	L	4C
VGS & RSAM	M	4D
STORE	N	4E
BAUD RATE	O	4F
RUN	P	50
CARRIAGE RETURN	CR	OD
HORIZONTAL TAB	HT	09
BACK SPACE	BS	08

NOTE: PRN, BPRN, STBY, REPEATER MODES ARE SELECTED VIA HORIZAONTAL TAB

Table 3.6b RS232-C Connector Pin-Outs

Pin No.	Circuit Mnemonic	Signal	Description
1	AA (GND)	Protective Ground	Not required. Can optionally be tied to analyzer chassis (earth ground)
2	BA (TX DTA)	Transmitted Data	Serial, asynchronous data from ATE to analyzer.
3	BB (RX DTA)	Received Data	Serial, asynchronous data from analyzer to ATE.
4	CA (RTS)	Request to Send	Sent by analyzer when it has a message ready to send.
5	CB (CTS)	Clear to Send	Sent to analyzer by ATE in response to Clear to send. The analyzer responds by sending a message.
6	CC	Data Set Ready	Not used
7	AB (Sig Gnd)	Signal Ground	Ground reference for all interface signals. Can optionally be tied to circuit AA.
8	CD (DCD)	Data Terminal Ready	Analyzer monitors this signal from ATE to determine if ATE system is on.

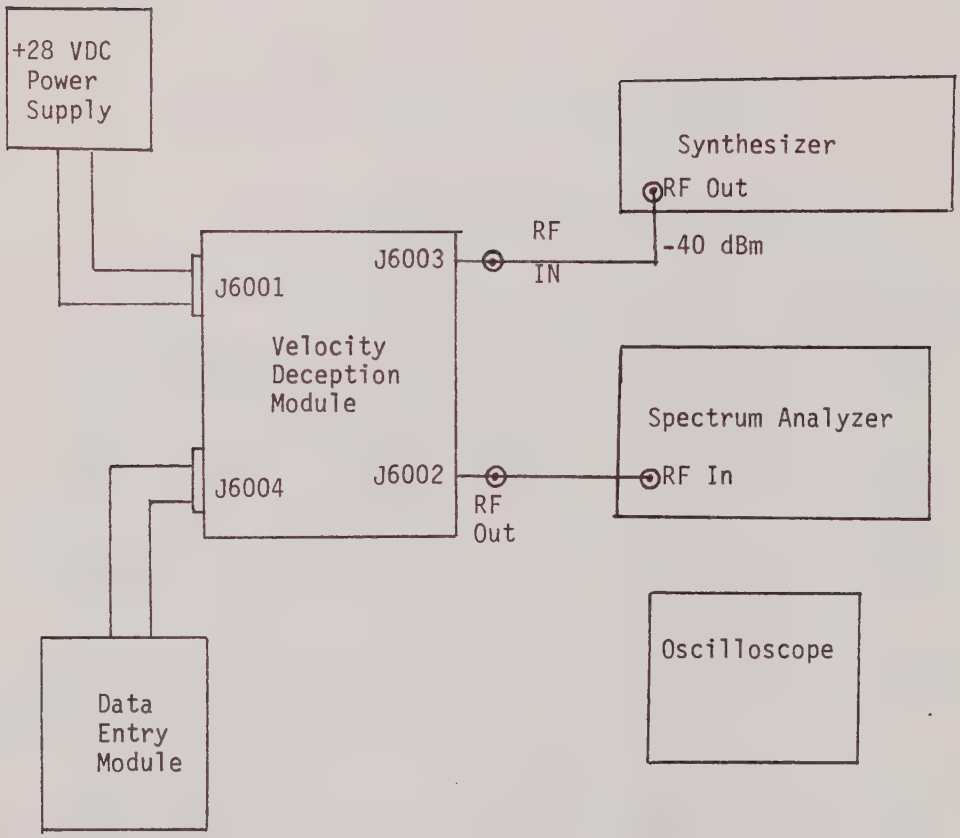


Figure 4.0: System Test Set-Up

4.0 SET UP AND TESTINGS (SERRODYNE AS A FREQUENCY TRANSLATOR)

4.1 INITIAL SET UP

Set up the VDA testings as follows: (Refer Figure 4.0)

a) Hook up the data entry module to VDA J6004 I/O Control.

b) Connect the DC Power supply with +28 VDC and GRD RET to pin 13 and 14 of the VDA J6001.

c) Connect the VDA RF input - J6003 to the synthesized signal source at -40 dBm and the VDA RF output -J6002 to the input of the spectrum analyzer. Set the tet frequency at 9000 MHz.

d) Turn the +28 VDC power supply on.

e) Observe a non serrodyne signal of 9000 MHz on the spectrum analyzer display and the data entry module reads "VDS IS READY". The numeric keypad is now disabled. Press any of the numeric keys or the $\overleftarrow{BS}$, $\overrightarrow{HT}$, RET and observe no change in display.

f) The system is now waiting for a function key. Depress one of the function keys and see it being displayed, e.g., VGS key display VGS MODE. Now at this point if any other function key is pressed, that mode will be displayed on the LCD. But if a numeric key is depressed, the LCD will read *VDS IS READY*. To accept a particular function key, depress the RET key when that mode is on LCD.

g) PROM & RESPONSE SEQUENCES

Follow the step by step instructions on Table 4.0 to verify the prom/response sequences.

4.2 SYSTEM TEST FOR VGS

4.2.1 Select VGS mode. Set SWP SRC = INT, TYPE = LINEAR, DIR SRC = INT, SWP DIR = CLOSE, WALK = 3 SECS, DWELL = .5 SECS, MAX DEV = 50 KHz. Run the VGS mode.

4.2.2 Verify all the sidebands within the 50 KHz of the translated carrier on the spectrum analyzer. It should be suppressed 20 dBc minimum. The carrier suppression should be greater than 20 dBc. The translation loss should be less than 4 dB at the frequency translation of 50 KHz $\pm$ 5% (see Figure 4.2.1).

4.2.3 Verify the VGS waveform on the oscilloscope at J60001-9 with respect to GROUND. The walk time should be at 3 secs $\pm$ 10%, the dwell time should be 0.5 secs $\pm$ 5%.

4.2.4 Monitor SERRO D/W test points at J6001-10 of the VDA. Verify the zero frequency on the oscilloscope during DWELL period and then starting point of VGS command which corresponds to the minimum VGS deviation. It should be <100 Hz or >10 msec (see Figure 4.2.2).

4.2.5 Repeat the above steps except entering TYPE = PARA. Verify the translated frequency in parabolic fashion on the spectrum analyzer.

4.2.6 Repeat step 4.2.1 except entering SWP DIR = OPEN. Verify the walk off direction is negative.

TABLE 4.0
VDM PARAMETERS ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
1	VGS	VGS MODE	N/A	SELECT VELOCITY GATE STEALER (VGS) MODE.
	RET		N/A	ACCEPT
		SWP SRC = INT	N/A	THE SYSTEM WILL GENERATE THE INTERNAL(INT) SWEEP SOURCE(SWP SRC)
	HT	SWP SRC = EXT/OFF	N/A	THE SYSTEM WILL USE THE EXTERNAL(EXT) SWEEP SOURCE.
	HT	SWP SRC = INT	N/A	BACK TO THE FIRST CHOICE OF INTERNAL SWEET SOURCE SELECTED
	RET		N/A	ACCEPTED INTERNAL SWEEP SOURCE .
2		TYPE = LINEAR	N/A	LINEAR WALK FUNCTION IS NOW AVAILABLE.
	HT	TYPE = PARA	N/A	PARABOLIC(PARA) TYPE WALK FUNCTION IS NOW AVAILABLE.
	HT	TYPE = LINEAR	N/A	LINEAR WALK FUNCTION IS SELECTED.
	RET			ACCEPTED LINEAR WALK FUNCTION .
3		DIR SRC = INT	N/A	THE DIRECTION (DIR) SOURCE(SRC) OF FREQUENCY TRANSLATION WILL BE CONTROLLED BY INTERNAL SIGNAL .
	HT	DIR SRC = EXT/OFF	N/A	THE DIRECTION (DIR) SOURCE(SRC) OF FREQUENCY TRANSLATION WILL BE CONTROLLED BY EXTERNAL SIGNAL
	HT	DIR SRC = INT	N/A	INTERNALLY CONTROLLED FREQUENCY TRANSLATION IS SELECTED.
	RET		N/A	ACCEPTED INTERNALLY CONTROLLED FREQUENCY TRANSLATION.
4		SWP DIR = OPEN	N/A	OPEN SWEEP(SWP)DIRECTION (DIR) OF FREQUENCY TRANSLATION IS NOW AVAILABLE .

TABLE 4.0 (cont.)
VDM PARAMETERS ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
	HT	SWP DIR = CLOSE	N/A	CLOSE DIRECTION (DIR) OF SWEEP (SWP) FREQUENCY TRANSLATION IS NOW AVAILABLE
	RET		N/A	CLOSE DIRECTION IS ACCEPTED.
5		WALK = 0.00 SEC	0.1 TO 25.5 SEC IN STEP OF .1 SEC	PROGRAM WALK TIME IN SECOND.
	2 7	WALK = 27 SEC	--	ENTER 27 THROUGHT THE KEYBOARD VALUE IS HIGHER
	RET	DATA ERROR HIGH	--	THAN LIMIT SET.
	RET	WALK = 0.00 SEC	--	BACK TO VALUE ENTER BEFORE.
	0 . 0 1	WALK = 0.01 SEC	--	VALUE INPUT 0.01 SEC IS ENTER.
	RET	DATA ERROR LOW	--	VALUE INPUT IS LOWER THAN LIMIT SET.
	RET	WALK = 0.00 SEC	--	BACK TO VALUE ENTER BEFORE.
	1	WALK = 1.00 SEC	--	VALUE INPUT 1 SEC IS ENTERED WITHIN THE SPECIFIED LIMIT.
	RET		--	1 SEC WALK TIME IS ACCEPTED.
6		DWELL = 0.00 SEC	0.5 TO 5 SEC IN STEP OF 0.05 SEC	PROGRAM DWELL TIME IN SECOND.
	. 5	DWELL = 0.5 SEC	--	VALUE INPUT 0.5 SEC IS ENTERED WITHIN THE LIMIT
	RET		--	0.5 SEC DWELL TIME IS ACCEPTED.
				NOTE *
7		MAX DEV = 0.0 KHZ	0.5 TO 127.5 KHZ IN STEP OF .5 KHZ	PROGRAM THE MAXIMUM(MAX) DEVIATION (DEV) IN KHZ.
	5 0	MAX DEV = 50 KHZ	--	VALUE INPUT 50 KHZ IS ENTERED WITHIN THE LIMIT
	RET			ACCEPTED 50 KHZ.
				NOTE *.
		* VDS IS READY *	N/A	ALL PARAMETERS AT VDS MODE HAVE BEEN ACCEPTED.

NOTE * : IF THE VALUE INPUT IS LOWER OR HIGHER THAN THE SPECIFIED LIMIT . THE MESSAGE ERROR LOW OR HIGH WILL APPEAR ON THE DISPLAY . HIT "RET" KEY TO RESET TO ORIGINAL VALUE .

TABLE 4.0 (cont.)

VDM PARAMETERS ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
8	NBRN	NBRN MODE	N/A	SELECT NARROW BAND REPEATER NOISE(NBRN) MODE.
	RET		N/A	PROGRAM NBRN MODE.
		MAX DEV = 0.0 KHZ	0.125 TO 32 KHZ IN STEP OF .125 KHZ.	PROGRAM THE MAXIMUM(MAX) FREQUENCY DEVIATION(DEV)
	2	MAX DEV = 2 KHZ		VALUE INPUT 2 KHZ IS ENTERED. NOTE *
	RET		N/A	ACCEPTED 2 KHZ.
		* VDS IS READY *		
9	RD	RANDOM MODE		SELECTED RANDOM DOPPLER MODE .
	RET	RDP TM = 0.0 MSEC	.2 TO 20 MSEC IN STEP OF .1 MSEC	
	1 0	RDP TM = 10 MSEC	--	ENTER 10 MSEC RANDOM DOPPLER (RDP) TIME (TM).
	RET		--	ACCEPTED 10 MSEC. NOTE *
10		MAX DEV = 0.0 KHZ	0.1 TO 25.5 KHZ	PROGRAM THE MAXIMUM(MAX) FREQUENCY DEVIATION(DEV)
	1 0	MAX DEV = 10 KHZ	--	ENTER 10 KHZ.
	RET		--	ACCEPTED 10 KHZ. NOTE *
		* VDS IS READY *		
11	HO&H	HO&H MODE	0.1 TO 25.5 SECS IN STEP OF .1 SEC	SELECTED HOLD-OUT (HO) AND HOOK (H) MODE.
	RET		--	
		HOLD = 0.0 SEC	--	PROGRAM HOLD TIME.
	1	HOLD = 1 SEC	--	1 SEC HOLD TIME IS ENTERED.
	RET		--	ACCEPTED 1 SEC HOLD TIME NOTE *
		* VDS IS READY *		
12	RSAM	RSAM MODE	N/A	SELECT REPEATER SWEPT AMPLITUDE MODULATION (RSAM) MODE .
	RET			
		MOD SRC = INT	N/A	INTERNAL SOURCE(SRC) AMPLITUDE MODULATIOM(MOD) CAN BE SELECTED.

NOTE * : IF THE VALUE INPUT IS LOWER OR HIGHER THAN THE SPECIFIED LIMIT . THE MESSAGE ERROR LOW OR HIGH WILL APPEAR ON THE DISPLAY . HIT "RET" KEY TO RESET TO ORIGINAL VALUE .

TABLE 4.0 (cont.)

VDM PARAMETERS ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
	HT	MOD SRC = EXT/OFF	N/A	EXTERNAL(EXT) AMPLITUDE MODULATION (MOD) SOURCE (SRC) CAN BE SELECTED .
	HT	MOD SRC = INT	N/A	BACK TO FIRST CHOICE.
	RET		--	INTERNAL SOURCE FOR RSAM HAS BEEN SELECTED.
13		SAM BEG = 0.0 HZ	5 TO 1275 HZ IN STEP OF 5 HZ.	SELECT THE BEGINNING (BEG) FREQUENCY OF SWEEP AMPLITUDE MODULATION (SAM) .
	5	SAM BEG = 5 HZ	--	5 HZ IS ENTERED.
	RET			ACCEPTED 5 HZ. NOTE *
		SAM END = 0 HZ	--	SELECT THE ENDING (END) FREQUENCY OF SWEEP AM- PLITUDE MODULATION (SAM)
	1 2 7 5	SAM END = 1275HZ	--	1275 HZ IS ENTERED.
	RET		--	ACCEPTED 1275 HZ. NOTE *
14		SAM SWP = 0.0 SEC	0.05 TO 12.75 SEC IN STEP OF.05 SEC	PROGRAM SWEEP AMPLITUDE MODULATION SWEEP (SWP) TIME .
	1	SAM SWP = 1 SEC	--	1 SEC RSAM SWEPT TIME IS ENTERED.
	RET		--	ACCEPTED 1 SEC. NOTE *
15		DUTY CYCLE = 0 %	10% TO 90% DUTY CYCLE IN STEP OF 5%.	PROGRAM RSAM DUTY CYCLE.
	5 0	DUTY CYCLE = 50%	--	ENTER 50% DUTY CYCLE.
	RET		--	ACCEPTED 50% DUTY CYCLE. NOTE *
		* VDS IS READY *		
16	MFR	MFR MODE	N/A	SELECT THE MULTIPLE FREQUENCY REPEATER (MFR) MODE .
	RET		N/A	
		MOD SRC = INT	N/A	SELECT INTERNAL (INT) SOURCE(SRC) OF AMPLITUDE MODULATION (MOD) .
	HT	MOD SRC = EXT/OFF	N/A	SELECT EXTERNAL (EXT) SOURCE(SRC) OF AMPLITUDE MODULATION (MOD) .
	HT	MOD SRC = INT	N/A	BACK TO FIRST CHOICE
	RET		N/A	ACCEPTED INTERNAL SOURCE

NOTE * : IF THE VALUE INPUT IS LOWER OR HIGHER THAN THE SPECIFIED LIMIT . THE MESSAGE ERROR LOW OR HIGH WILL APPEAR ON THE DISPLAY . HIT "RET" KEY TO RESET TO ORIGINAL VALUE .

TABLE 4.0 (cont.)

VDM PARAMETERS ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
17		MFR FQ = 0.0 HZ	10 TO 2550 HZ IN STEP OF 10 HZ.	SELECT THE FREQUENCY(FQ) OF MULTIPLE FREQUENCY REPEATER (MFR) MODE .
	1 0 0 RET	MFR FQ = 100 HZ	-- N/A	ENTER 100 HZ . ACCEPTED 100 HZ . NOTE *
		DUTY CYCLE = 0.0%	10% TO 90% IN STEP OF 5%	PROGRAM THE MFR DUTY CYCLE.
	5 0	DUTY CYCLE = 50 %	--	ENTER 50% DUTY CYCLE.
	RET		--	ACCEPTED 50% DUTY CYCLE. NOTE *
		* VDS IS READY *		
19	VGS & RSAM	VGS & RSAM MODE	N/A	SELECT THE VELOCITY GATE STEALER (VGS) & RANDOM SWEEP AMPLITUDE MODULATION MODE (RSAM) .
	RET		N/A	PROGRAM THE VGS & RSAM MODE.
		SWP TM = 0.0 SEC	0.05 TO 12.75 SEC IN STEP OF.05 SEC	PROGRAM THE RSAM SWEEP (SWP) TIME (TM) OF THIS MODE .
	5	SWP TM = 5 SEC	--	ENTER 5 SEC SWEPT TIME.
	RET		--	ACCEPTED 5 SEC . NOTE *
		SAM TRG = 0 KHZ	0.5 TO 127.5 KHZ IN STEP OF .5 KHZ	SELECT THE SWEEP AMPLITUDE MODULATION (SAM) TRIGGER (TRG) FREQUENCY.
	4 0	SAM TRG = 40 KHZ	--	ENTER 40 KHZ TRIGGER FREQUENCY .
	RET			ACCEPTED 40 KHZ . NOTE *
		* VDS IS READY *		
21	STORE	STORE	--	STORE ALL PARAMETERS.
	RET	* VDS IS READY *	--	ALL PARAMETERS HAVE BEEN STORED .

NOTE * : IF THE VALUE INPUT IS LOWER OR HIGHER THAN THE SPECIFIED LIMIT . THE MESSAGE ERROR LOW OR HIGH WIIL APPEAR ON THE DISPLAY . HIT "RET" KEY TO RESET TO ORIGINAL VALUE .

TABLE 4.0 (cont.)
VDM PARAMETRES ENTRY PROMPTS/RESPONSES

STEP	KEY	MESSAGE DISPLAY	SPECIFICATION	EXPLANATION
22	RS232	RS232 SETUP MODE	N/A	SELECT RS2E2 BAUD RATE.
	RET	BAUD RATE = 50	--	PROGRAM BAUD RATE.
	HT	BAUD RATE = 75	--	ONCE PRESSING THE "HT" KEY , EACH VALUE OF BAUD RATE IS BEING DISPLAYED. THE SYSTEM IS CAPABLE COMMUNICATING WITH THE HOST COMPUTER AT THE PARTICULAR BAUD RATE .
	HT	BAUD RATE = 134.5		
		:		
		:		
	RET		--	ACCEPTED SELECT BAUD RATE .
		* VDS IS READY *		
23	RUN / STOP	RUN MODE	N/A	SELECT PARTICULAR MODE FOR RUNNING.
	RET	STANDBY MODE	N/A	THE FIRST RUN MODE IS DISPLAYED . ONCE
	HT	VGS MODE	N/A	PRESSING THE "HT" KEY , EACH MODE WILL APPEAR
	HT	NBRN MODE	N/A	ON DISPLAY .PARTICULAR MODE CAN BE SELECTED TO
	HT	RANDOM MODE	N/A	RUN WHEN HIT THE "RET" KEY THE DISPLAY SHOWS A
	HT	PRN MODE	N/A	" VDS RUNNING " MESSAGE. AT THIS POINT ALL KEYS
	HT	VGS & RSAM MODE	N/A	ARE DISABLED EXCEPT THE RUN/STOP KEY.THE ONLY
	HT	HO & H MODE	N/A	WAY TO STOP RUNNING IS TO HIT THIS KEY AGAIN.
	HT	RSAM MODE	N/A	NOW THE SYSTEM BACK TO READY.
	HT	MFR MODE	N/A	
	HT	REPEATER MODE	N/A	
	HT	BLINKING PRN MODE	N/A	
	HT	COUNT DOWN BLINK	N/A	
	RET	VDS RUNNING		RUN THE SELECTED MODE .
	RUN / STOP			STOP RUNNING MODE .
	RET	* VDS IS READY *		

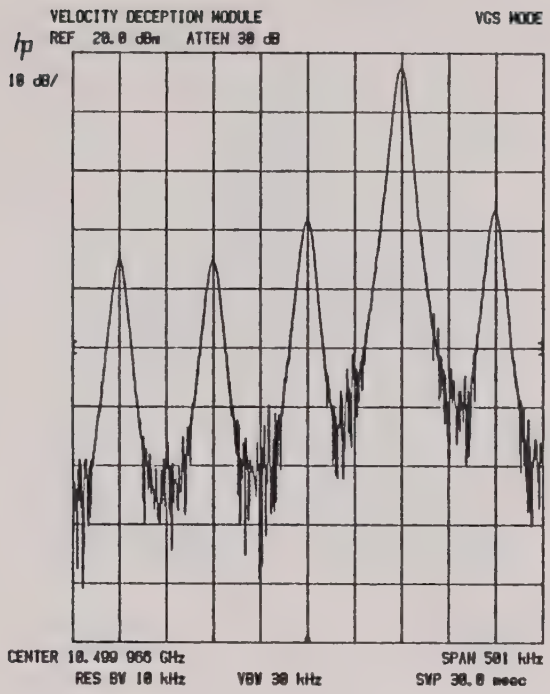


Figure 4.2.1: Typical VDA Velocity Gate Stealer (VGS) and Hold Out & Hook(HOH) Spectrum

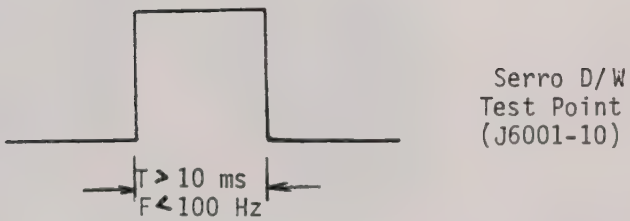


Figure 4.2.2: Typical Serro D/W Waveform

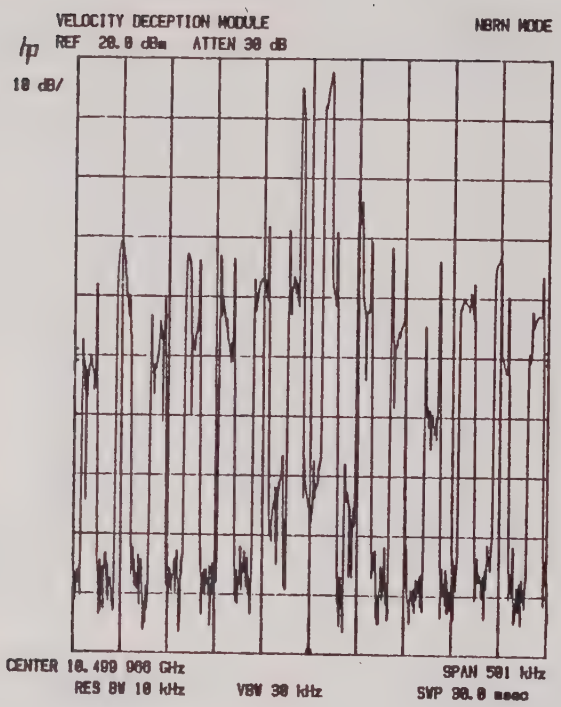


Figure 4.3: Typical VDA Narrow Band Repeater Noise (NBRN) Spectrum

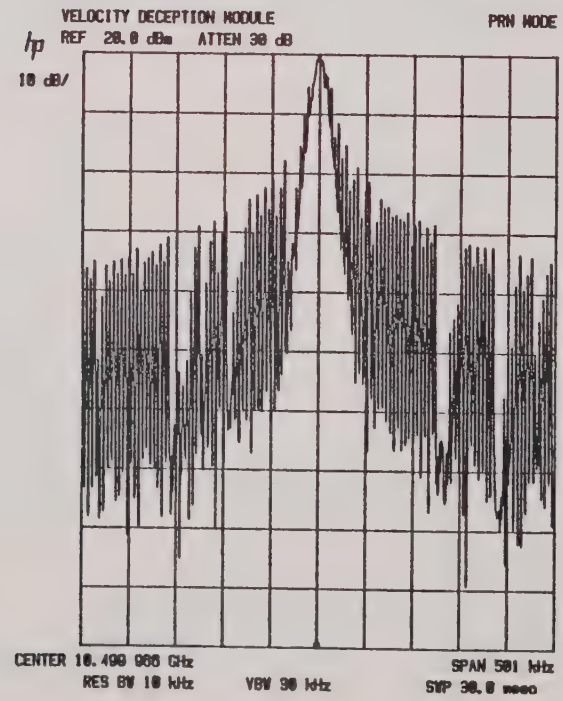


Figure 4.5: Typical VDA Pseudo Ramdom Noise (PRN) Spectrum

4.3 SYSTEM TEST FOR NBRN MODE

4.3.1 Select NBRN mode. Set MAX DEV = 32 KHz and run NBRN modes. Verify the NBRN response of 32 KHz $\pm$ 5% with the insertion loss <3 dB on the spectrum analyzer (see Figure 4.3).

4.3.2 Select NBRN mode. Set MAX DEV = % KHz and run NBRN mode. Verify the NBRN response of 5 KHz $\pm$ 10% with the insertion loss <3 dB on the spectrum analyzer.

NOTE: There is also a fixed AM 450 Hz, 40% duty cycle in this NBRN mode.

4.4 SYSTEM TEST FOR RD MODE

4.4.1 Select RD mode. Set RDPTM = 20 msec. MAX DEV = 25.5 KHz and run RD mode.

4.4.2 Verify the RD response on the spectrum anlayzer. The maximum deviation should be within 25.5 KHz $\pm$ 5%. The translation loss should be $\leq$ 3 dB.

4.4.3 Verify the Random Doppler Time of 20 msec generated at J6001-9 on the oscilloscope.

4.4.4 Set RDPTM = .200 msec. Verify the random doppler time of 200 μ secs generated at J6001-9 on the oscilloscope.

4.5 SYSTEM TEST FOR PRN & BPRN MODES

NOTE: The bandwidth of PRN and BPRN modes is programmable from 50 Hz to 5 KHz through random doppler time of RD mode from 20 msecs to .200 msecs.

4.5.1 Select RD mode. Set RDPTM = .200 msecs. Then run PRN mode. Verify the PRN response with the bandwidth of 5 KHz on the spectrum analyzer. (See Figure 4.5).

4.5.2 Repeat Step 4.5.1 except entering RDPTM = 1 msec. Verify the PRN response with the bandwidth of 1 KHz on the spectrum analyzer.

4.5.3 Select MFR mode and set MFRFQ = 200 Hz. Run BPRN mode. Verify the PRN response with the blinking time of 0.5 secs on the spectrum analyzer.

4.6 SYSTEM TEST FOR RSAM MODE

4.6.1 Select RSAM mode. Set MOD SRC = INT, SAMBEG = 5 HZ, SAMEND = 1275 Hz, SAM SWP = .05 sec, DUTY CYCLE = 10%.

4.6.2 Run RSAM mode. Verify the RSAM frequency response, the depth of RF modulation (> 50 dBc) with the duty cycle of 10%. (See Figure 4.6)

4.6.3 Repeat the above step except entering DUTY CYUCLE = 90%. Verify the RSAM frequency response with the duty cycle of 90%.

4.7 SYSTEM TEST FOR VGS AND RSAM MODE

4.7.1 Select VGS mode, set SWP SRC = INT, TYPE = LINEAR, DIR SRC = INT, SWP DIR = CLOSE, WALK = 10 SECS, DWELL = 1 SECS, MAX DEV = 50 KHz.

4.7.2 Select RSAM mode, set MOD SRC = INT, SAM BEG = 5 Hz, SAM END = 1275 Hz, SAM SWP = 2 SECS, DUTY CYCLE = 50%.

4.7.3 Select VGS & RSAM MODE, set SWPTIM = 2 SECS, SAM TRIG = 10 KHz. Run the VGS & RSAM mode. Verify the combination reponse VGS & RSAM on the spectrum analyzer as follows: The sweep time 2 secs with the SAM TRIG at 10 KHz, the insertion loss <4.0 dB and 50 dB RF depth modulation.

4.7.4 Repeat the steps 4.7.1, 4.7.2 except entering MAX DEV = 100 KHz.

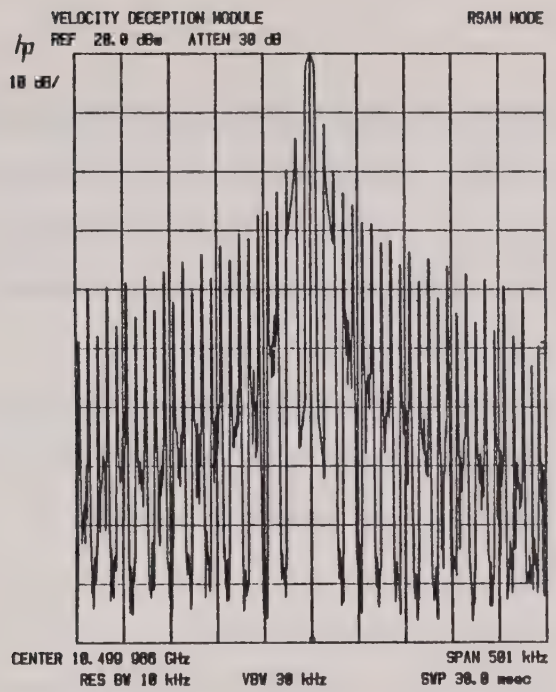


Figure 4.6: Typical VDA Repeater Swept Amplitude Modulation (RSAM Spectrum)

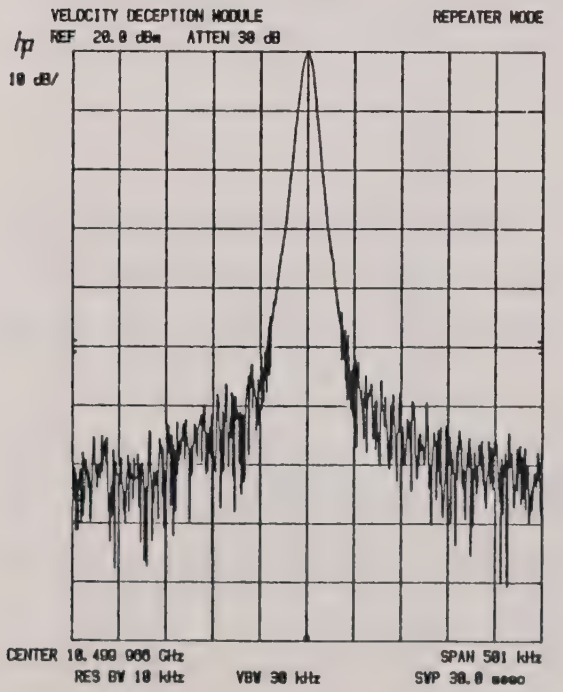


Figure 4.10a: Typical VDA Repeater (RPTR) Spectrum

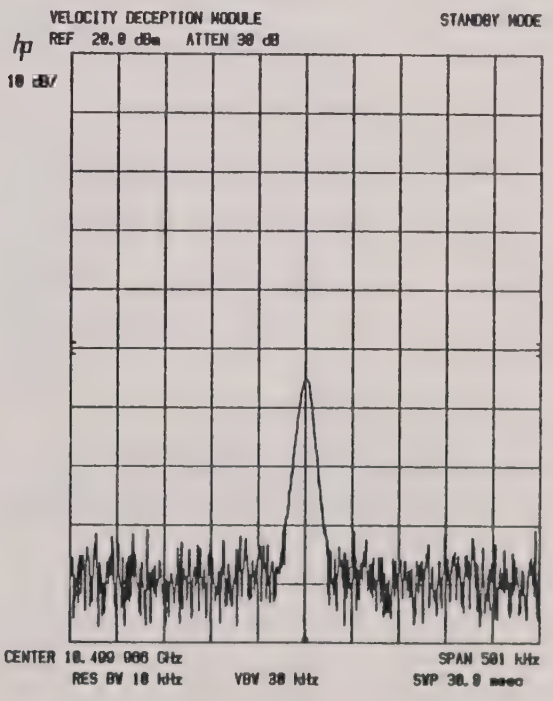


Figure 4.10b: Typical VDA Standby (STBY) Spectrum

4.7.5 Select VGS & RSAM mode, set SWPTM = 2 SECS, SAM TRIG = 50 KHz. Run the VGS & RSAM mode. Verify the combination response VGS & RSAM on the spectrum analyzer as follows: the SAM Trigger at 50 KHz with the sweep time of 2 secs, the worst case insertion loss <9 dB and 50 dB RF depth modulation.

4.8 SYSTEM TEST FOR MFR AND CDB MODE

4.8.1 Select MFR mode, set MOD SRC = INT, MFRFQ = 10 Hz, DUTY CYCLE = 10%. Run the MFR mode. Verify the MFR signal on the spectrum anlayzer: the depth of RF modulation of 50 dB minimum with the modulation frequency of 10 Hz, 10% duty cycle.

4.8.2 Set MFRFQ = 1000 Hz and select CDB mode. Verify the CDB response of 10 Hz on the spectrum anlayzer. (1/100 of MFR frequency).

4.8.3 Repeat Step 4.8.1 except entering MFRFQ = 2550 Hz, DUTY CYCLE = 90%. Run the MFR mode. Verify the depth of RF modulation of 50 dB minimum with the modulation frequency of 2550 Hz, 90% duty cycle on the spectrum analyzer.

4.9 SYSTEM TEST FOR HOH MODE

4.9.1 Set VGS mode at WALK = 5 SECS, DWELL = 3 SECS, MAX DEV = 127.5 KHz. Select HO&H mode, set HOLD = 25.5 seconds and run HO&H mode. Verify the hold time on the spectrum analyzer, it should be 25.5 seconds $\pm$ 5%.

4.9.2 Repeat step 4.9.1 except entering WALK = 3 SECS, DWELL = 1 SEC. Set HOLD = 3 secs and run HO&H mode. Verify the hold out time of 3 secs on the spectrum analyzer. Figure 4.2.1 shows the typical response for HOH mode on the spectrum analyzer.

4.10 SYSTEM TEST FOR STBY AND REPEATER MODE

4.10.1 Run REPEATER mode. Verify the non-serrodyne signal on the spectrum analyzer. (See Figure 4.10a)

4.10.2 Run STBY mode. Verify the RF Signal attenuates >50 dBc on the spectrum analyzer. (See Figure 4.10b)

4.11 THE COMMANDS AND MONITOR FUNCTIONS CHECK

4.11.1 After all parameters are entered via data entry module, hit STORE, RET Key. Now all the parameters are stored in the NOVRAM of the VDA.

4.11.2 Turn the power supply OFF and disconnect the data entry module from the VDA.

4.11.3 Turn the power supply on again and verify the TTL command code A, B, C, D through J6001 pin 2,3,4,5 as follows:

A B C D	MODE
0 0 0 0	STBY
1 0 0 0	VGS
0 1 0 0	NBRN
1 1 0 0	RD
0 0 1 0	PRN
1 0 1 0	VGS & RSAM
0 1 1 0	HO&H
1 1 1 0	RSAM
0 0 0 1	MFR
1 0 0 1	REPEATER
0 1 0 1	BPRN
1 1 0 1	CDB

NOTE: The +5V and ground return is available at J6001-18 and 14. A pull-up resistor of 3K is recommended to use for TTL control.

4.12 EXTERNAL CONTROL CHECK

4.12.1 Verify the EXTERNAL U/D CONTROL (OPEN/CLOSE) at VGS mode by selecting DIR SRC = EXT/OFF. Switch the external U/D TTL control at J6001-9.

Verify the positive and negative translation on spectrum anlayzer.

4.12.2 Verify the EXTERNAL SWEEP SOURCE at VGS mode by selecting SWP SRC = EXT/OFF. Inject a DC signal to EXT TRANS control at J6001-8. Verify the fix frequency translation on the spectrum analyzer.

4.12.3 Verify the EXTERNAL AM AT MFR mode by selecting MOD SRC = EXT. Inject a TTL signal between 10 to 2550 Hz, 50% duty cycle. Verify the MFR response on the spectrum analyzer with this EXTERNAL AM control.

4.13 SUPPORT EQUIPMENT

TEST EQUIPMENT	CHARACTERISTICS REQUIRED
1. Synthesized Signal Generator Systron Donner SD1626	.100 - 26 GHz frequency range, low spurious and phase noise, +8 to -99 dbm calibrated output through step attenuator, internal level pulse modulation.
2. DC Power Supply Systron Donner HB-50-3	0-50 Volts; 0-3 Amps
3. Digital Multimeter Systron Donner SD 7205	Ranges: ± 0.100000 V, ± 1.00000 V, ± 10.0000 V, ± 100.000 V and ± 1000.00 V. resolution: ± 1 μ V to ± 0.01 V in decade steps (depending on range). Overrange: 30% except 1000 V range. Maximum readings, ± .13000 V, ± 1.30000 V, ± 13.0000 V, ± 130.000 V and ± 10000.00 V at full accuracy.
4. VDM Test Fixtrue Systron Donner TF#313573-01	Control TTL Logic Command for various deception modes, and external control, monitor.
5. Function Generator Systron Donner SD401	Frequency Range .1 to 2 Hz, X 1 to X 1M; 20 Vpp. Max output, 50/600 Ω ; narrow/wide offset adjust.
6. Plotter Hewlett Packard HP7470A	Resolution: Smallest addressable step size: 0.025 mm (0.001 in) Repeatability: With a given pen: 0.1 mm From pen to pen: 0.2 mm Acceleration: 2 g's typical Plotting Area: X-Axis: 191 mm Y-Axis: 257 mm HB-1B Interfaces (IEEE 488-1978)
7. Spectrum analyzer Hewlett Packard HP8566B	Frequency Measurement Range: 100 Hz to 22 GHz with internal mixer, dc coupled input, synthesizer frequency accuracy, direct plot capability. Amplitude Measurement Range" -134 to +30 dBm Calibration: Log = 10 dB/dov for 90 dB display from Ref. level 5 dB/div for 50 dB display from Ref. level 2 dB/div for 20 dB display from Ref. level 1 dB/div for 10 dB display from ref. level Linear: 10% of Ref. level/div in voltage

8.	Power Meter Hewlett Packard HP 436A	Frequency Range: 100 KHz to 26.5 GHz Power Range (with 8485A sensor): 50 dB with 5 full scale ranges of -20, -10, 0, 10 and 20 dBm Accuracy: ± .0.02 dB ± 0.001 dB/°C
9.	Storage Oscilloscope Tektronik TEK 466	100 Mhz Portable Storage 5 ^{mv}/div, 5^{ns}/div Sweep Rate with 10x Sweep magnifier, 3000 div/$_{ns}$ stored writing speed.

NOTE: The above equipments are recommended by Systron Donner. Howerver, they could be replaced by an equivalent type of equipment as available.

5.0: VDA TROUBLESHOOTING

Figure	Logic Diagrams
5. 0	VDA Overall Troubleshooting
5. 1	Power Supply Trouble Isolation
5. 2	DEM Display Trouble Isolation
5. 3	Test Modes Trouble Isolation
5. 4	VGS Mode Trouble Isolation
5. 5	NBRN Mode Trouble Isolation
5. 6	RD Mode Trouble Isolation
5. 7	PRN & BPRN Mode Trouble Isolation
5. 8	RSAM Mode Trouble Isolation
5. 9	VGS & RSAM Mode Trouble Isolation
5.10	MFR Mode Trouble Isolation
5.11	HOH Mode Trouble Isolation
5.12	STBY Mode Trouble Isolation
5.13	REPEATER Mode Trouble Isolation
5.14	EXT. CONTROL Trouble Isolation

	Schematics
5.15	VDA Overall Block Diagram
5.16	Interconnect Diagram
5.17	Wiring Diagram
5.18	Power Supply Schematic
5.19	Digital P.C.B. Schematic
5.20	Analog P.C.B. Schematic
5.21	Interface Module Schematic

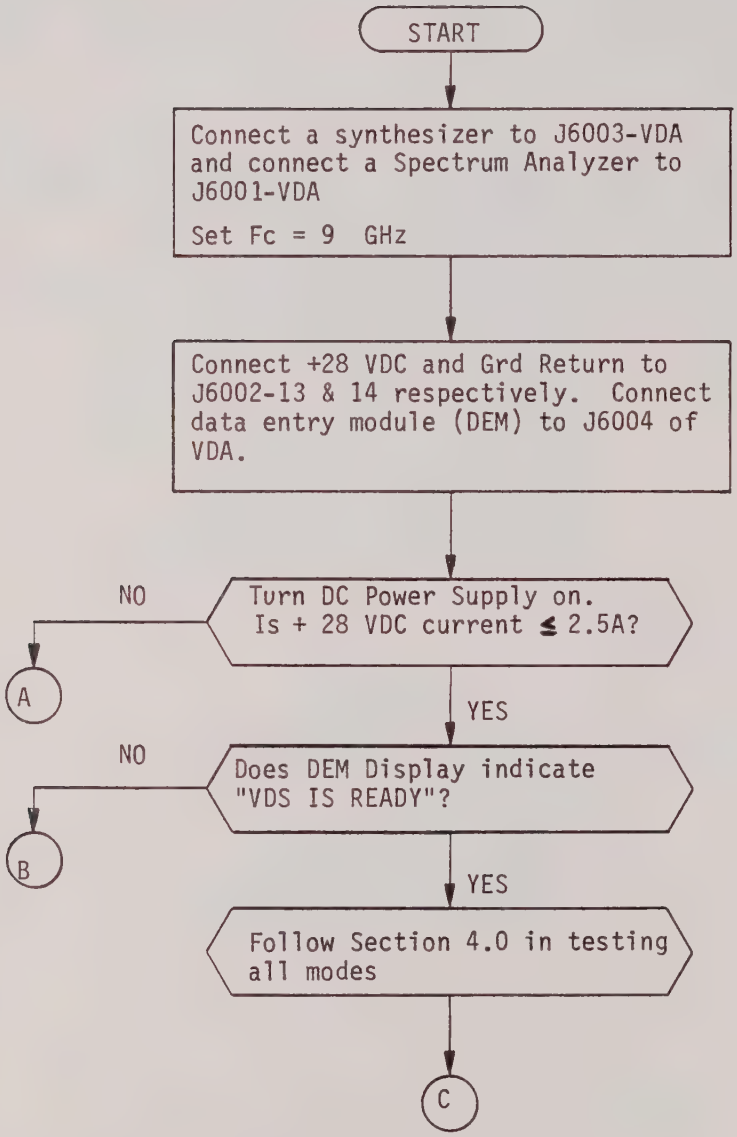

START
Connect a synthesizer to J6003-VDA and connect a Spectrum Analyzer to J6001-VDA
Set Fc = 9 GHz
Connect +28 VDC and Grd Return to J6002-13 & 14 respectively. Connect data entry module (DEM) to J6004 of VDA.
Turn DC Power Supply on. Is + 28 VDC current ≤ 2.5A?
NO
A
YES
Does DEM Display indicate "VDS IS READY"?
NO
B
YES
Follow Section 4.0 in testing all modes
C

Figure 5.0: Overall Troubleshooting

Figure 5.1: Power Supply Trouble Isolation

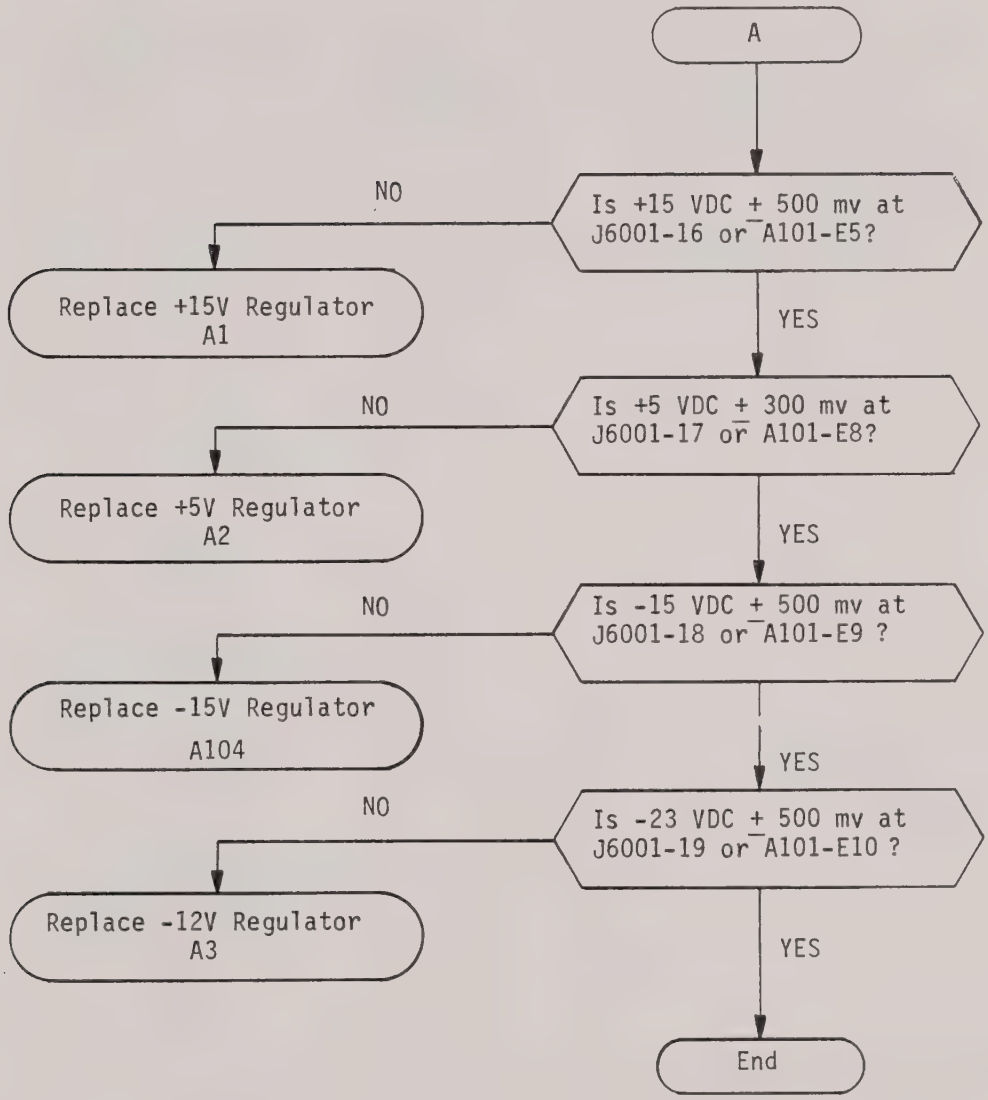
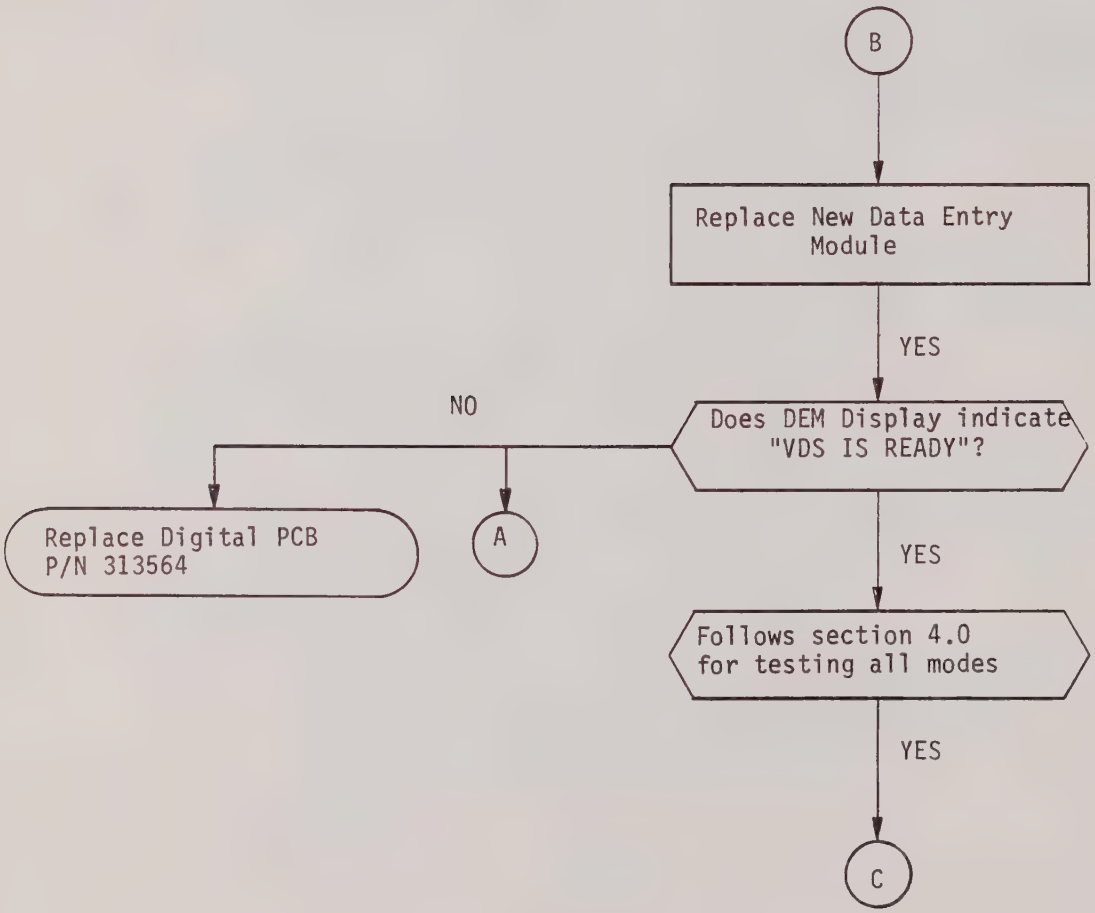


Figure 5.2: Trouble Isolation for Data Entry Module Display



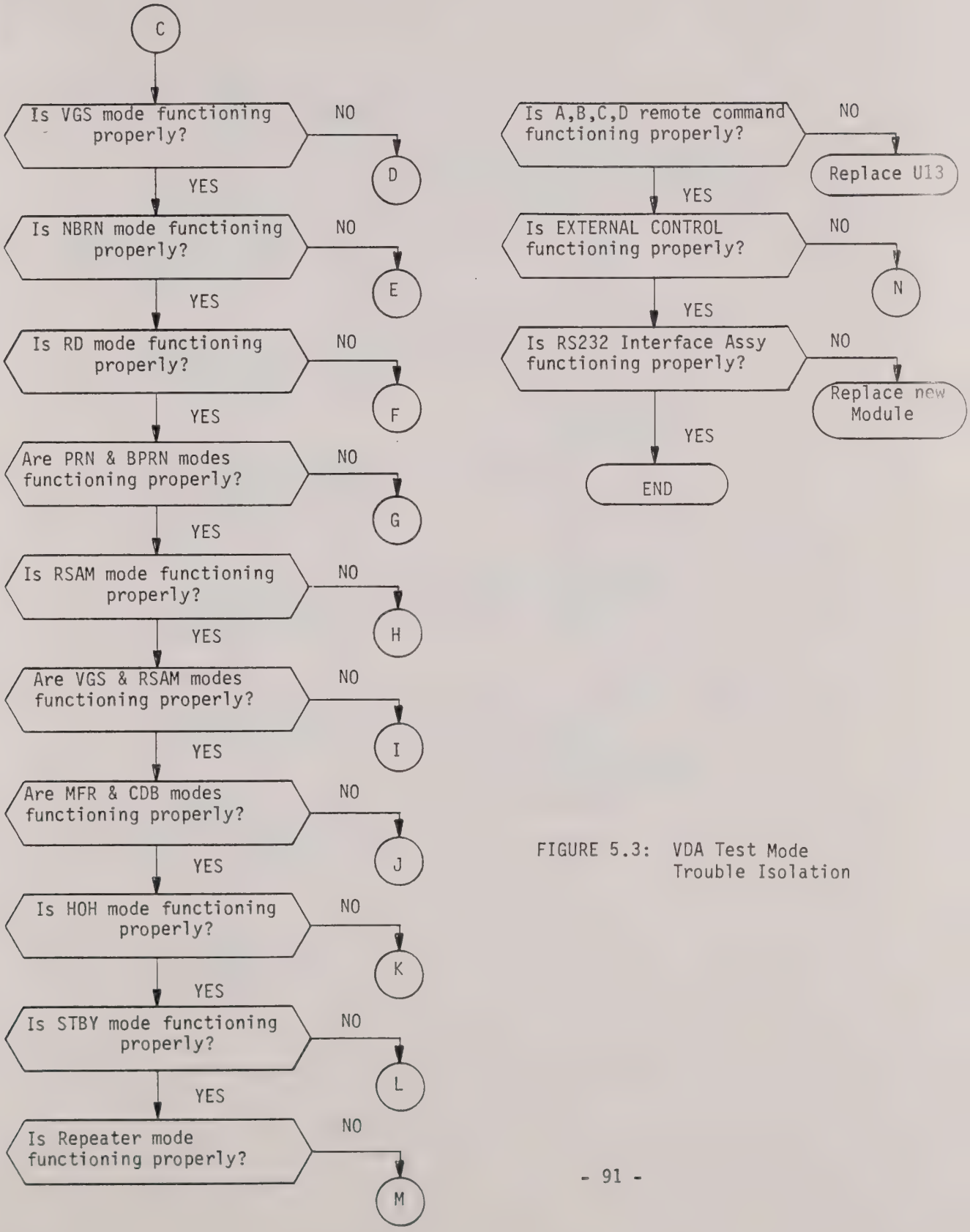


FIGURE 5.3: VDA Test Mode Trouble Isolation

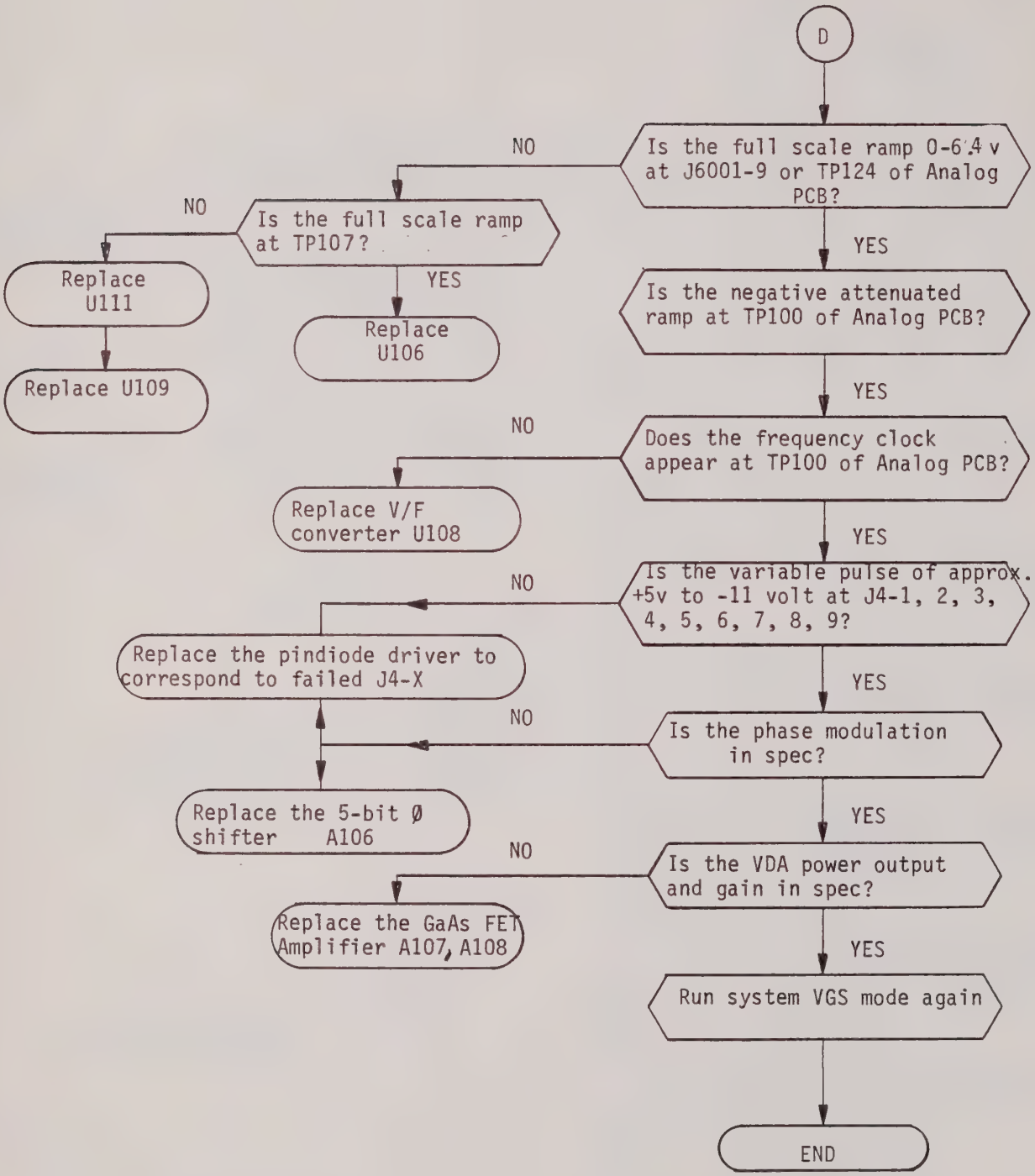

D
Is the full scale ramp 0-6.4 v at J6001-9 or TP124 of Analog PCB?
NO
Is the full scale ramp at TP107?
NO
Replace U111
Replace U109
YES
Replace U106
YES
Is the negative attenuated ramp at TP100 of Analog PCB?
YES
Does the frequency clock appear at TP100 of Analog PCB?
NO
Replace V/F converter U108
YES
Is the variable pulse of approx. +5v to -11 volt at J4-1, 2, 3, 4, 5, 6, 7, 8, 9?
NO
Replace the pindiode driver to correspond to failed J4-X
YES
Is the phase modulation in spec?
NO
Replace the 5-bit Ø shifter A106
YES
Is the VDA power output and gain in spec?
NO
Replace the GaAs FET Amplifier A107, A108
YES
Run system VGS mode again
END

Figure 5.4: VGS Mode Trouble Isolation

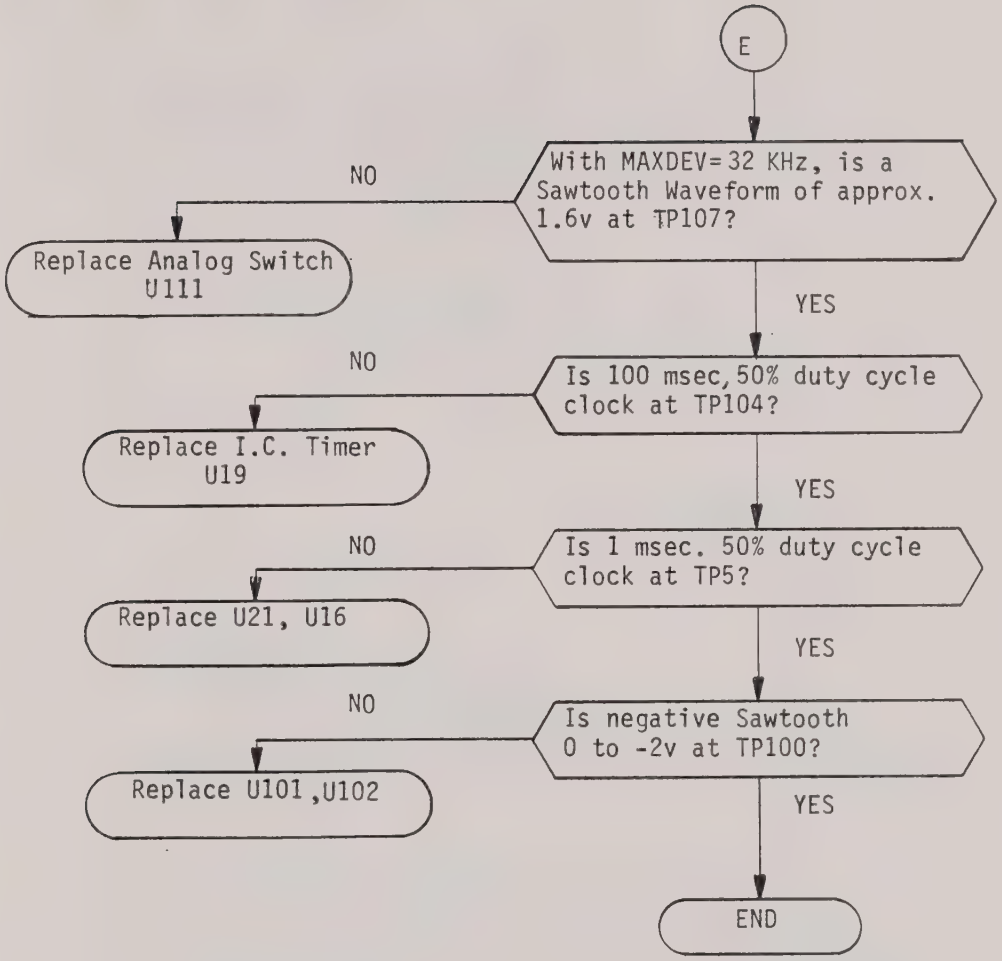


Figure 5.5: NBRN Mode Trouble Isolation

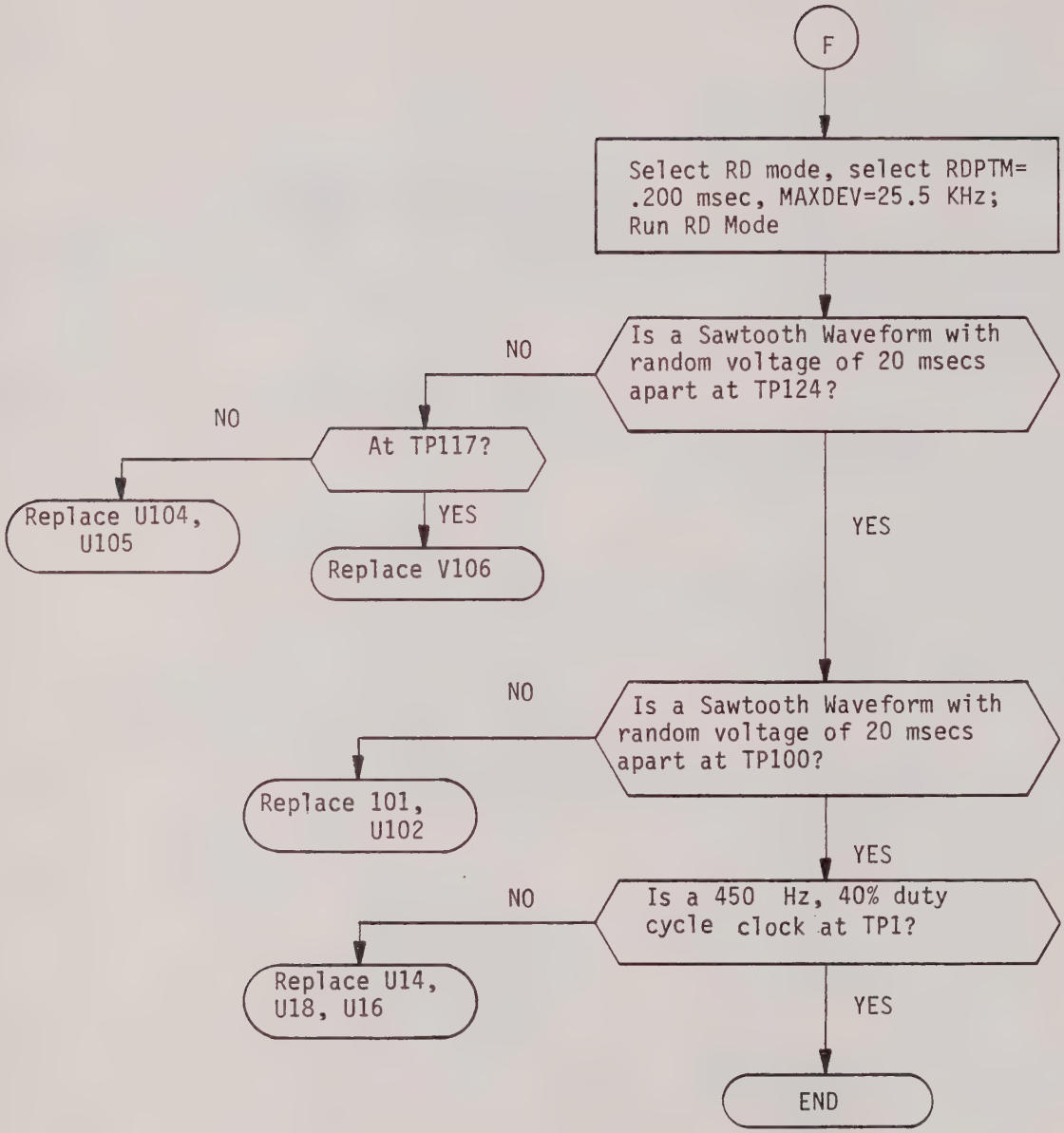


Figure 5.6: RD Trouble Isolation

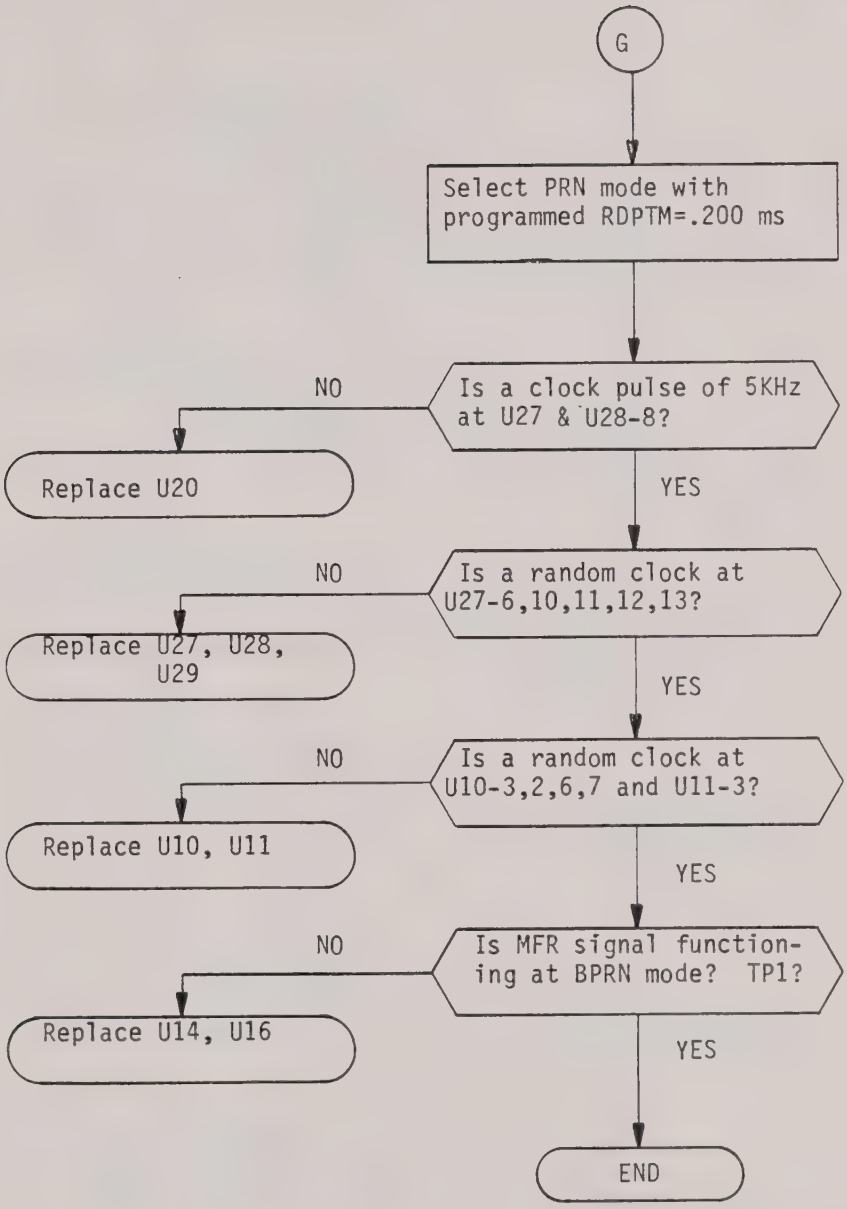


Figure 5.7: PRN &BPRN Mode Trouble Isolation

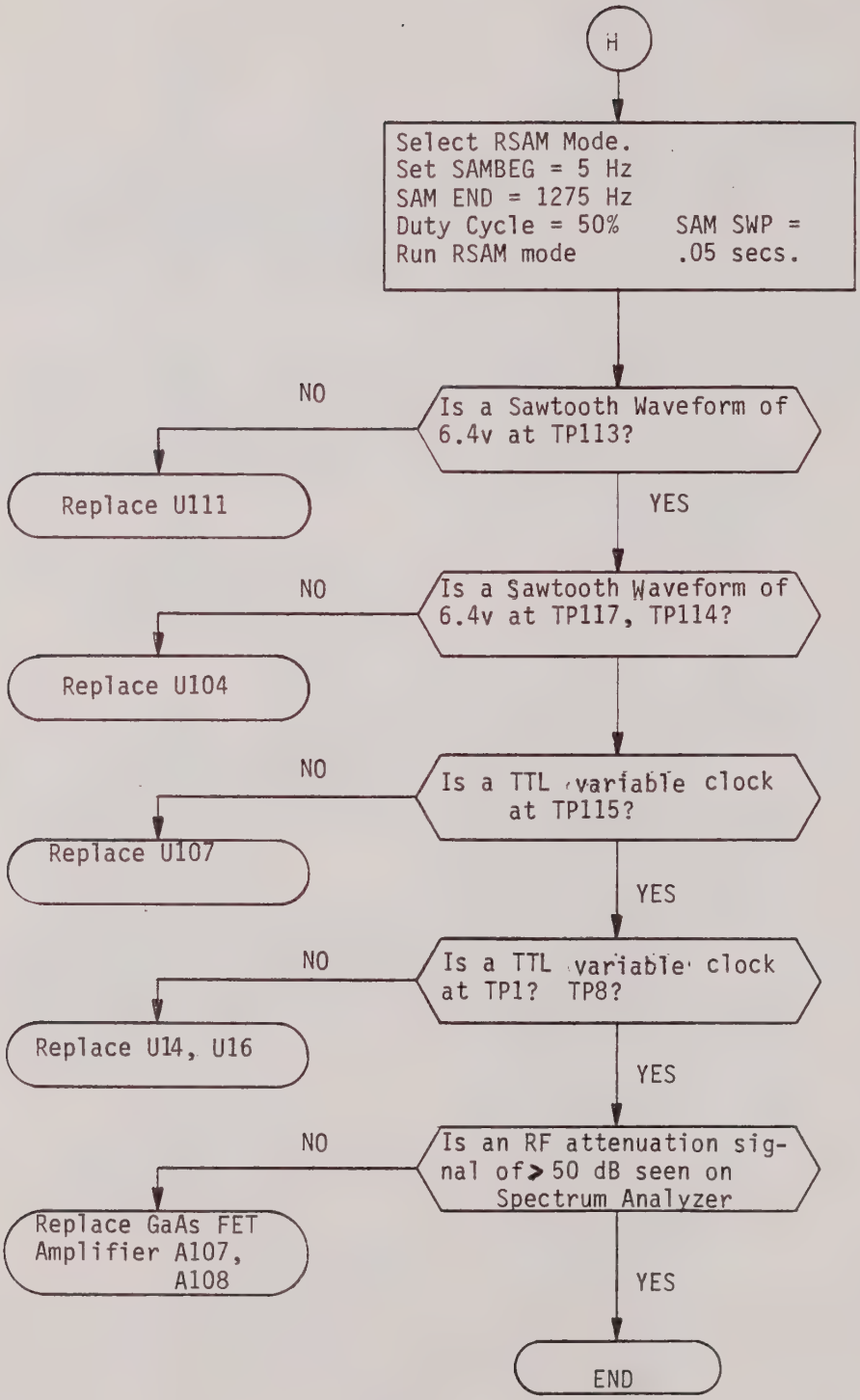


Figure 5.8: RSAM Mode Trouble Isolation

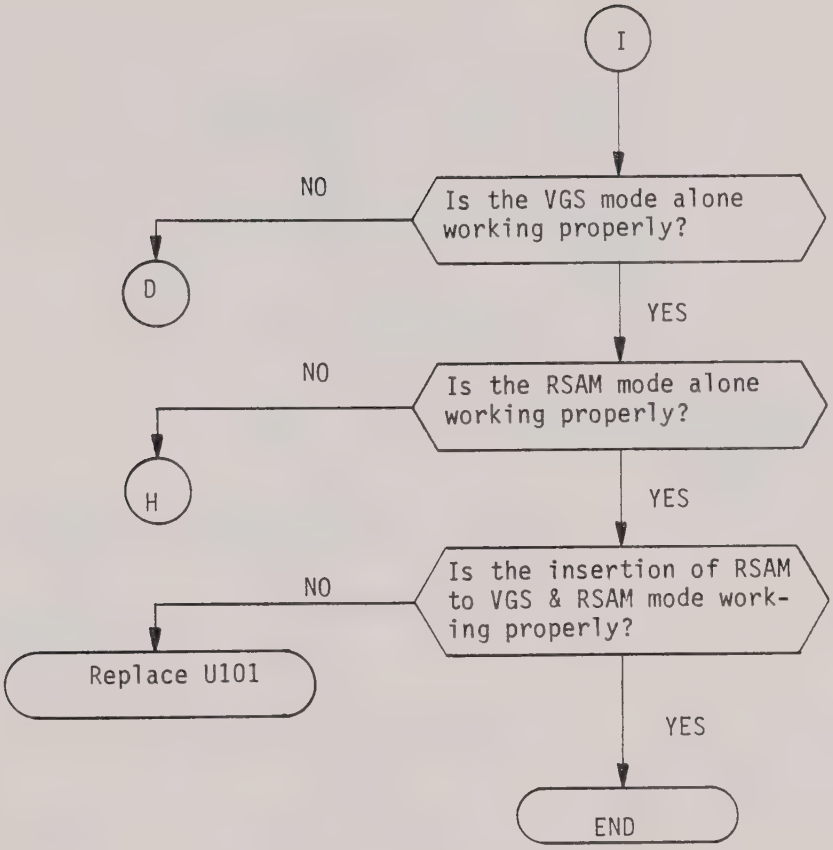


Figure 5.9: VGS & RSAM Mode Trouble Isolation

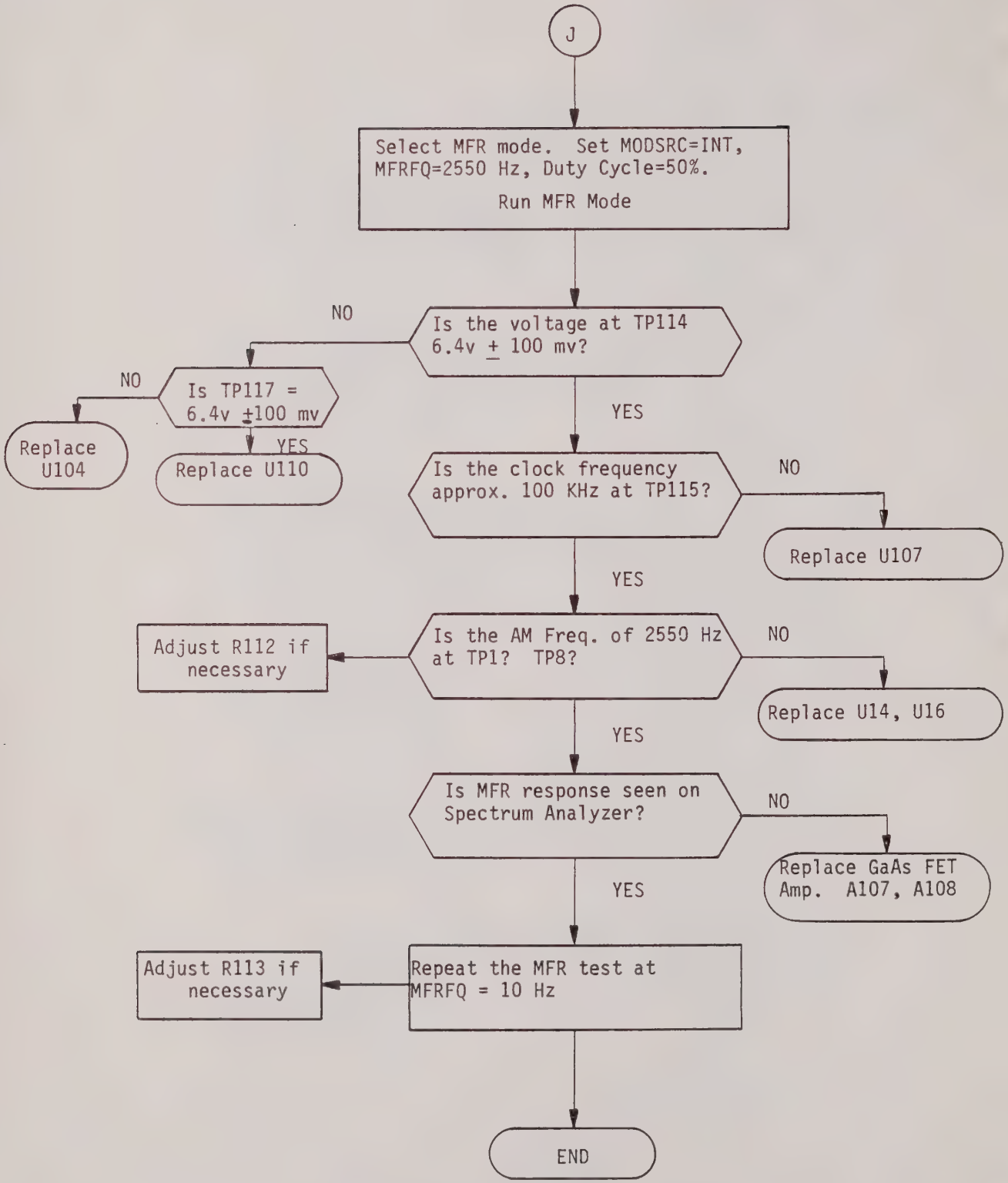


Figure 5.10: MFR Mode Trouble Isolation

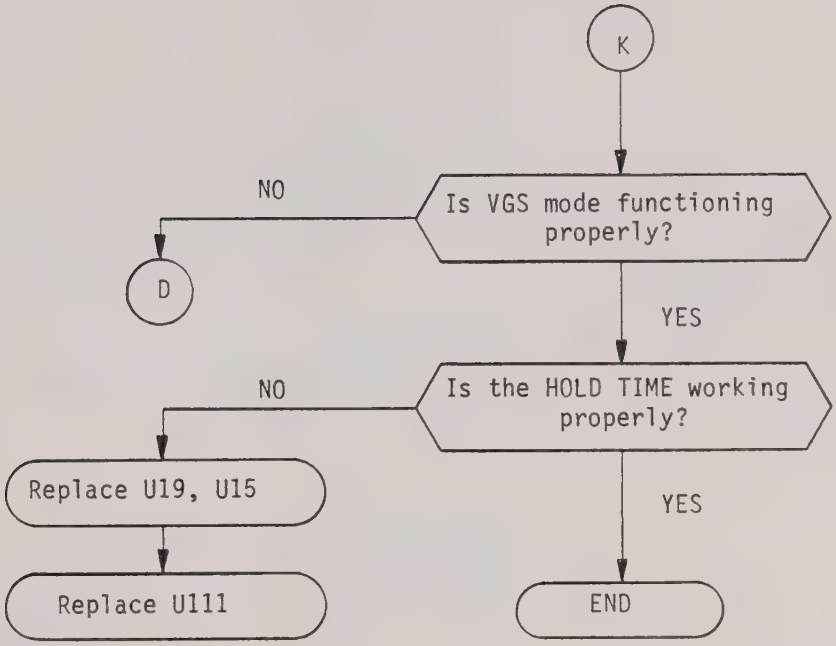


Figure 5.11: HOH Mode Trouble Isolation

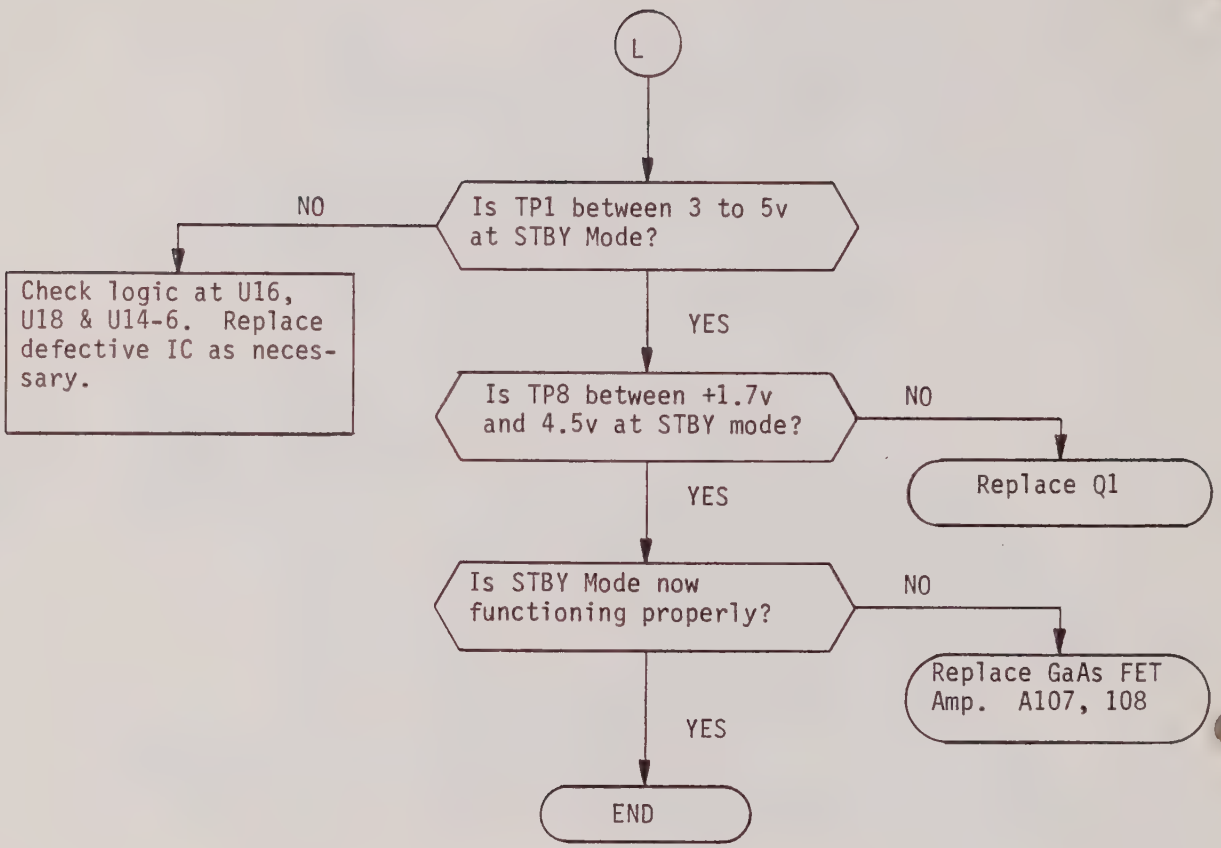


Figure 5:12 STBY Mode Trouble Isolation

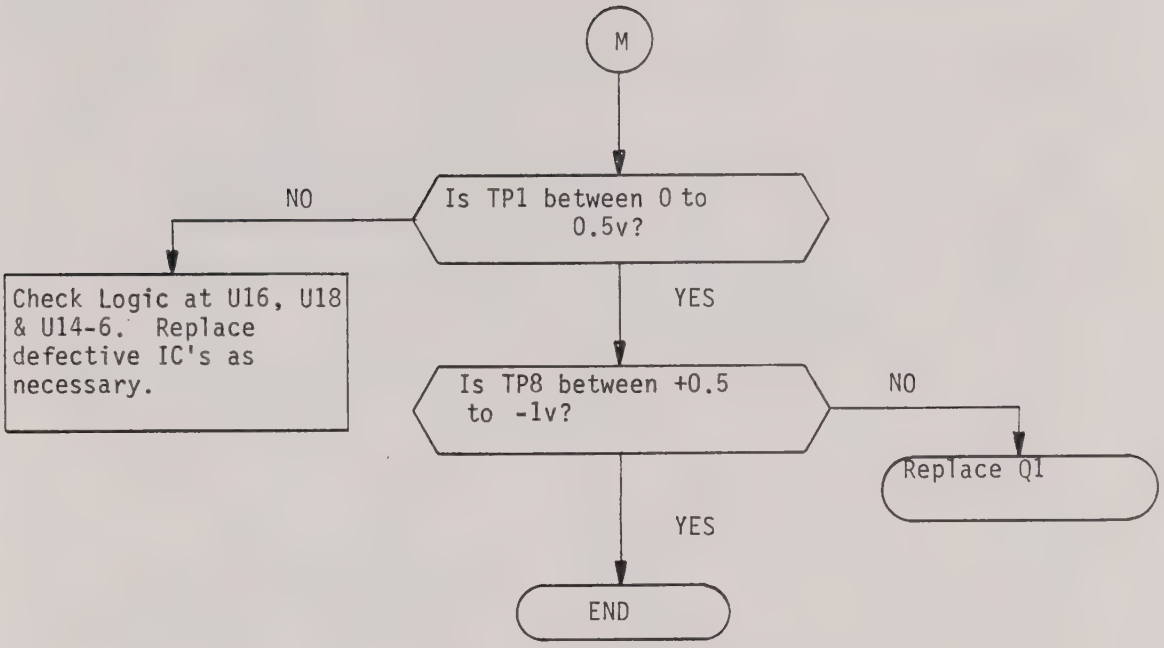


Figure 5.13: Repeater Mode Trouble Isolation

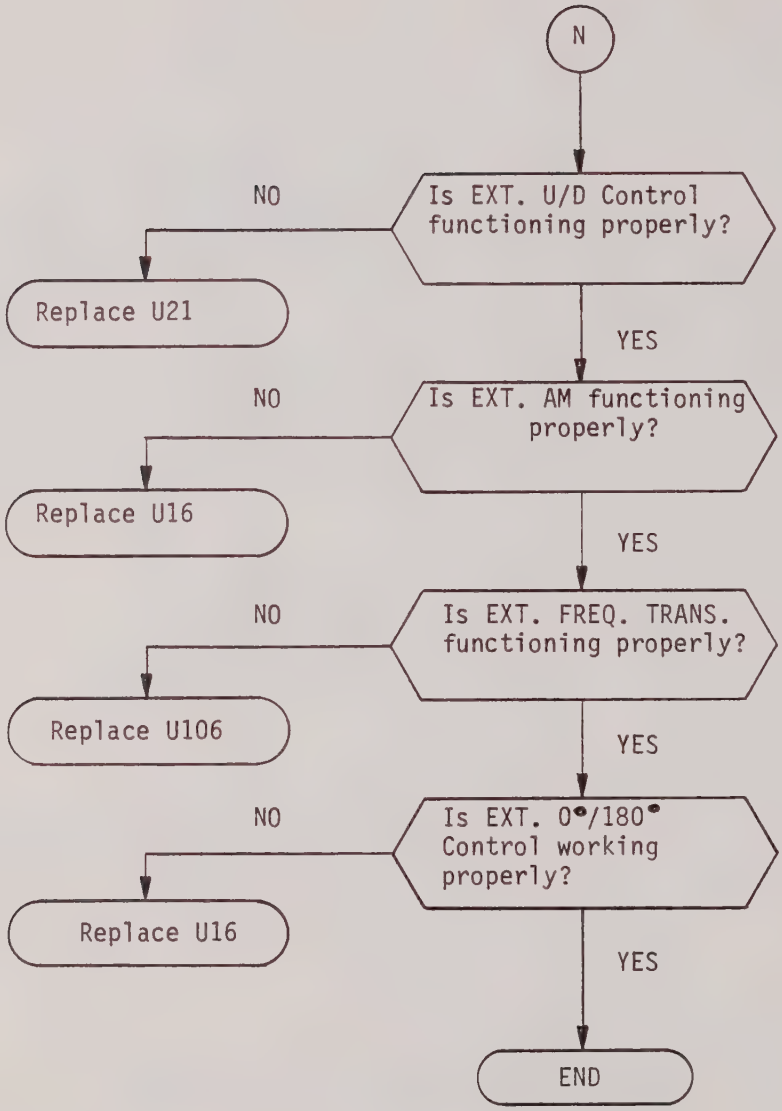


FIGURE 5.14: External Control Trouble Isolation

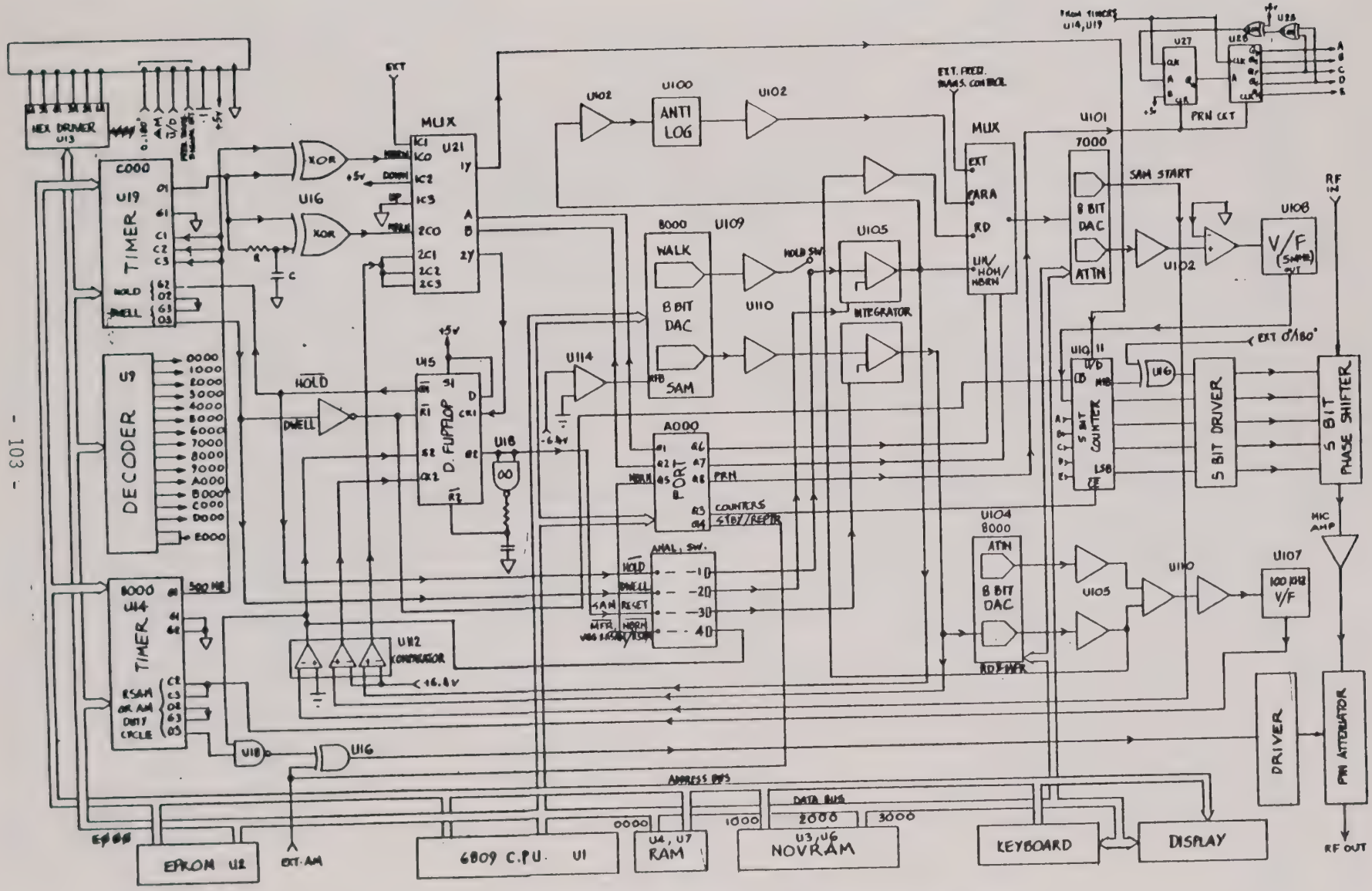


Figure 5.15 Detail Block Diagram of Solid State Deception Module

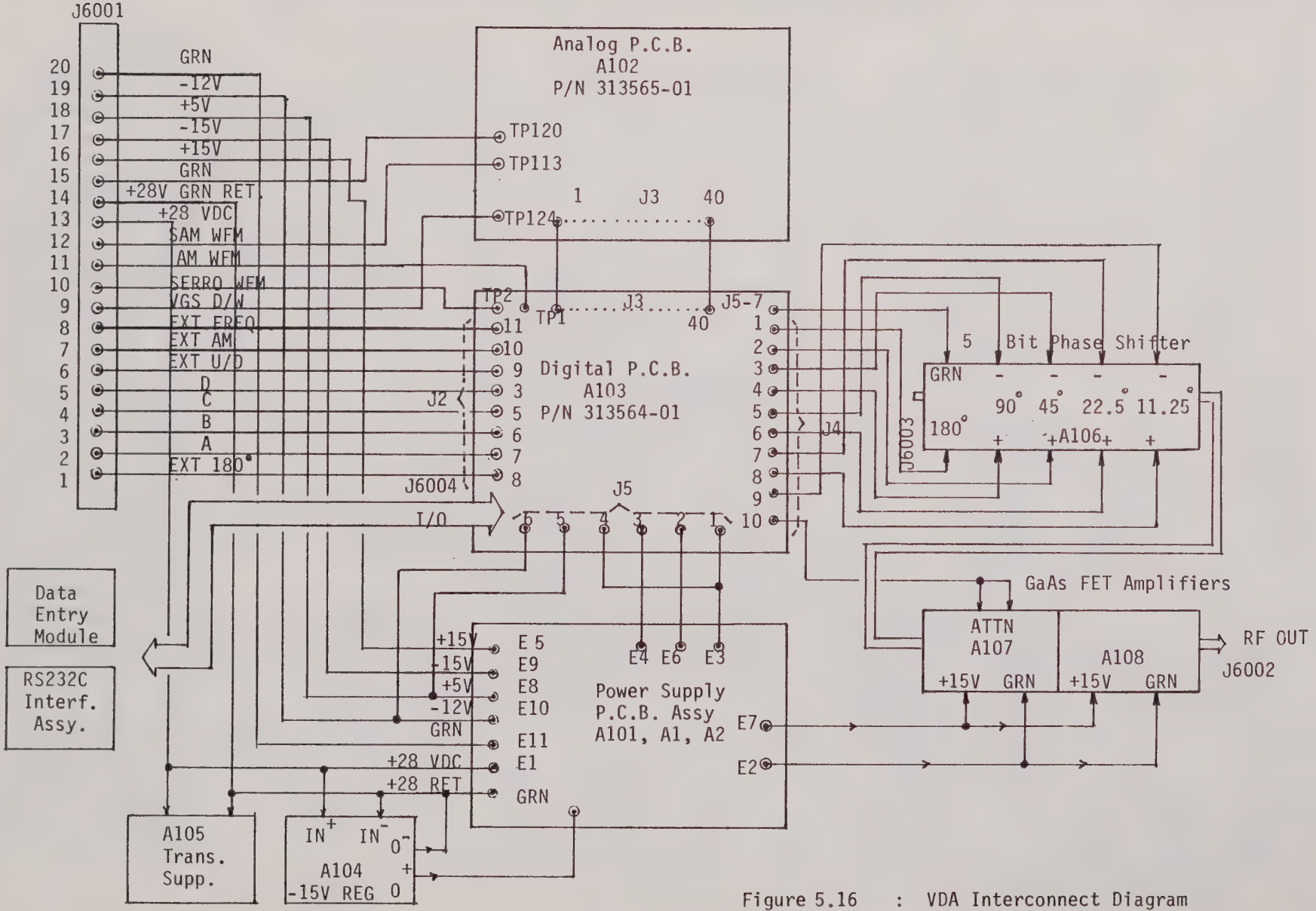


Figure 5.16 : VDA Interconnect Diagram

FIGURE 5.17

	WIRE LIST	LIST NO.	REV
		WL 312068-01	B

ASSEMBLY Velocity Deception Module	BY	DATE	SHEET 1 OF 2
MECH ASSY DWG NO	DRN		APPROVED
PART OF	CHK		
WIRING PROCESS SPECIFICATION	ENG Thang Vu	3-18-88	

WIRE NO.	GA.	IDENT COLOR	FROM COMPONENT	FROM PIN	TO COMPONENT	TO PIN	LENGTH (IN.)	REMARKS
1	24	Wht/Blk	J6001	1	A103-J2	8	9½	Ext. 0°/180°Control
2	24	Wht/Brn	J6001	2	A103-J2	7	9½	Command 'A' Control
3	24	Wht/Red	J6001	3	A103-J2	6	9½	Command 'B' Control
4	24	Wht/Org	J6001	4	A103-J2	5	9½	Command 'C' Control
5	24	Wht/Yel	J6001	5	A103-J2	3	9½	Command 'D' Control
6	24	Wht/Grn	J6001	6	A103-J2	9	10	Ext U/D Control
7	24	Wht/Blu	J6001	7	A103-J2	10	10	Ext AM Control
8	24	Wht/Vio	J6001	8	A103-J2	11	10	Ext Freq. Trans. Control
9	24	Wht/Gry	J6001	9	A102	TP 124	16½	Monitor VGS Dwell/Walk
10	24	Wht/Blk/Blu	J6001	10	A103	TP 2	12	Monitor Serro Waveform
11	24	Wht/Blk/Red	J6001	11	A103	TP 1	12	Monitor AM Waveform
12	24	Wht/Blk/Grn	J6001	12	A102	TP 113	16½	Monitor SAM Waveform
13	24	Blu	J6001	13	A105	+	4	+28 V (Input)
14	24	Blk	J6001	14	A105	-	4	GND (Input)
15	24	Blk	J6001	15	A102	TP 120	18	GND (Return)
16	24	Org	J6001	16	A101	E5	8¼	+15 V
17	24	Vio	J6001	17	A101	E9	9¼	-15 V
18	22	Red	J6001	18	A101	E8	8½	+5 V
19	24	Yel	J6001	19	A101	E10	9½	-12 V
20	24	Blk	J6001	20	A101	E11	9 3/4	GND
21	--	---	J6001	21	--	--	----	----
22	--	---	J6001	22	--	--	----	----
24	24	Org	A101	E7	A107	+15V	8	+15 V
25	24	Blk	A101	E2	A107	GND	8	GND

Figure 5.17 (cont.)

ASSY – Velocity Deception Module	WIRE LIST NO.	REV	SHEET
	WL312068-01	B	2 OF 2

WIRE NO.	GA.	IDENT COLOR	FROM		TO		LENGTH (IN.)	REMARKS
			COMPONENT	PIN	COMPONENT	PIN		
26	24	Org	A101	E7	A108	+15 V	8	+15 V
27	24	Blk	A101	E2	A108	GND	8	GND
28	22	Buss	A107	ATT	A107	ATT	3/4	ATT
29	24	Wht/Brn	A103-J4	1	A106	A180°	12½	180° (+)
30	24	Wht/Org	A103-J4	2	A106	A45°	12 3/4	45° (+)
31	24	Wht/Yel	A103-J4	3	A106	B45°	13 ¼	45° (-)
32	24	Wht/Red	A103-J4	4	A106	A90°	13 ¼	90° (+)
33	24	Wht/Blk	A103-J4	5	A106	B90°	13 ¼	90° (-)
34	24	Wht/Vio	A103-J4	6	A106	A22.5°	15 ½	25.5° (+)
35	24	Wht/Grn	A103-J4	7	A106	B22.5°	14 ½	22.5° (-)
36	24	Wht/Gry	A103-J4	8	A106	A11.25°	15 ¼	11.25° (+)
37	24	Wht/Blu	A103-J4	9	A106	B11.25°	13 3/4	11.25° (-)
38	24	Wht/Blk/Blu	A103-J4	10	A107	ATT	15 ¼	Attenuator Pin
39	24							
40	24	Blk	A103-J5	1	A101	E3	12	GND
41	24	Org	A103-J5	2	A101	E6	11 ¼	+15 V
42	24	V10	A103-J5	3	A101	E4	12 ½	-15 V
43	24	Blk	A103-55	4	A101	E3	12	GND
44	22	Red	A103-J5	5	A101	E8	11 ½	+5 V
45	24	Yel	A103-J5	6	A101	E10	12 3/4	-12 V
46	24	Blk	A103-J5	7	A106	GND	12 ½	GND
47	24							
48	24	Blu	A104	IN+	A101	E1	3	+28 V (Input)
49	24	Blk	A104	IN-	A101	GND LUG	3	GND (28 V Return)
50	24	Vio	A104	OUT-	A101	E4	3	-15 V
51	24	Blk	A104	OUT+	A101	E11	4	GND (-15 V Return)
52	24	Blu	A105	+	A104	IN+	4	+28 V (Input)
53	24	Blk	A105	-	A104	IN-	4	GND (28 V Return)

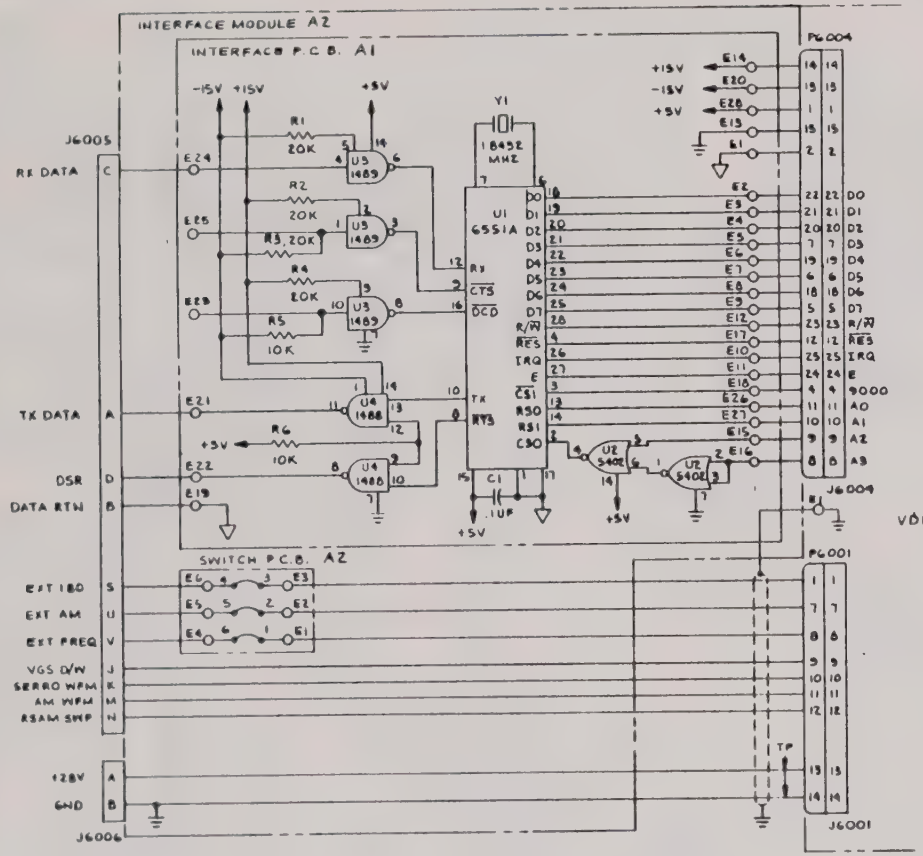


FIGURE 5.18

NOTES:
1. CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 50V.
2. RESISTOR VALUES ARE IN OHMS, ±1%, 1/4 W.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL PER EO18402		

9314072	00314072
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

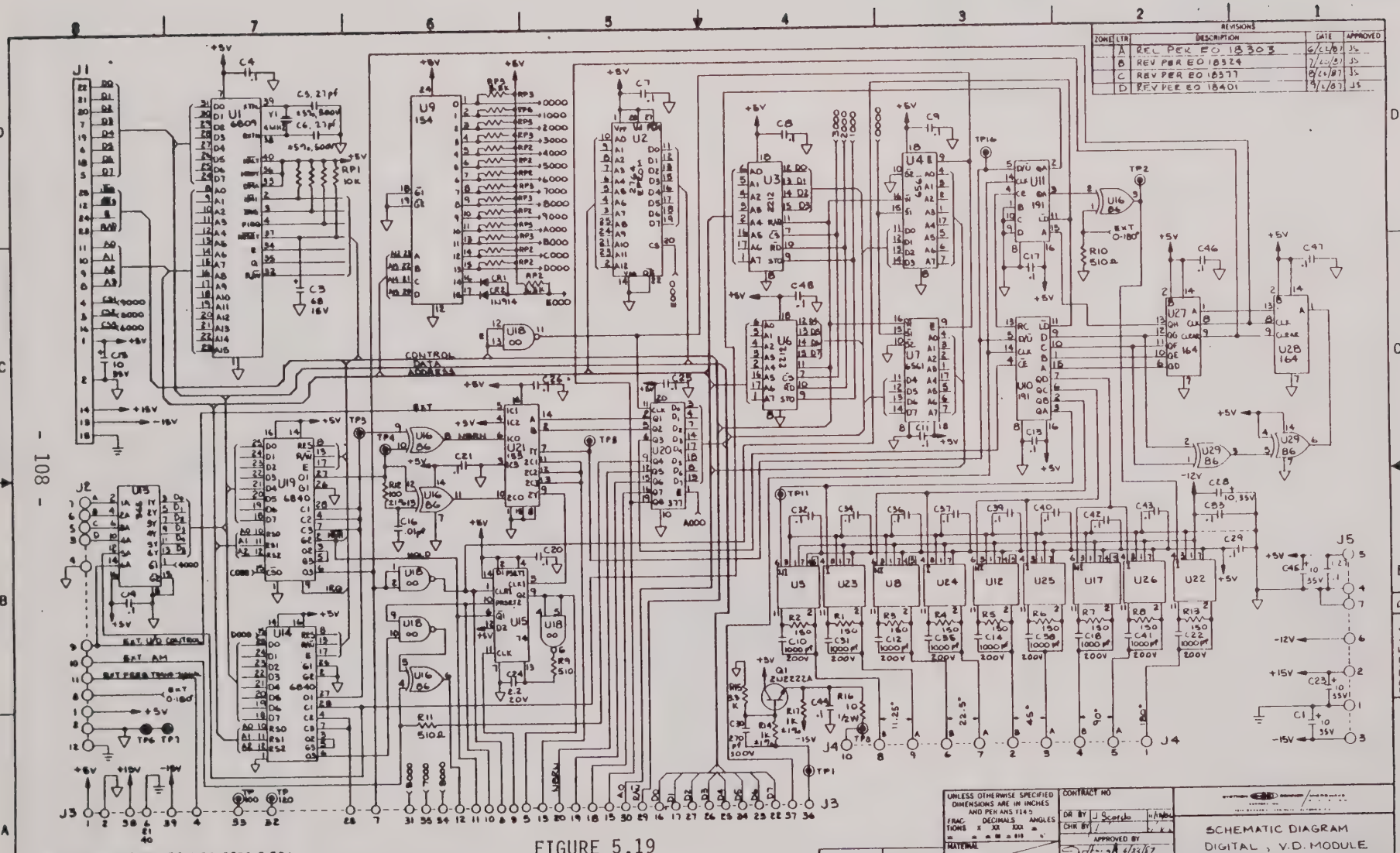
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND PER ANSI Y14.5
FINISH: DECIMALS ANGLES TOLERANCES .X ±.01 .XXX ±
MATERIAL
FINISH
CONTRACT NO.
DR BY
CHK BY
APPROVED BY

SCHEMATIC, INTERFACE MODULE

SIZE	CODE IDENT NO.	DWG NO.
D	01220	7D314072

SCALE —
SHEET OF

7D312072 A


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REL PER EO 18303 6/24/87 JS
B REV PER EO 18324 7/22/87 JS
C REV PER EO 18377 8/24/87 JS
D REV PER EO 18401 9/1/87 JS
CONTROL DATA ADDRESS
NOTES - UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE IN OHMS ± 2%, 1/4W.
2. CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 50V.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND PER ANSI Y14.5
CONTRACT NO
DR BY J Scordo
CHK BY
APPROVED BY
MATERIAL
FINISH
DO NOT SCALE DRAWING
SCHEMATIC DIAGRAM
DIGITAL , V.D. MODULE
SIZE D
CODE IDENT NO 01220
DWG NO 7D313564
SCALE
SHEET 1 OF 1
313564-01 VDM
NEXT ASSY USED ON
APPLICATION
FIGURE 5.19
- 108 -
7D313564

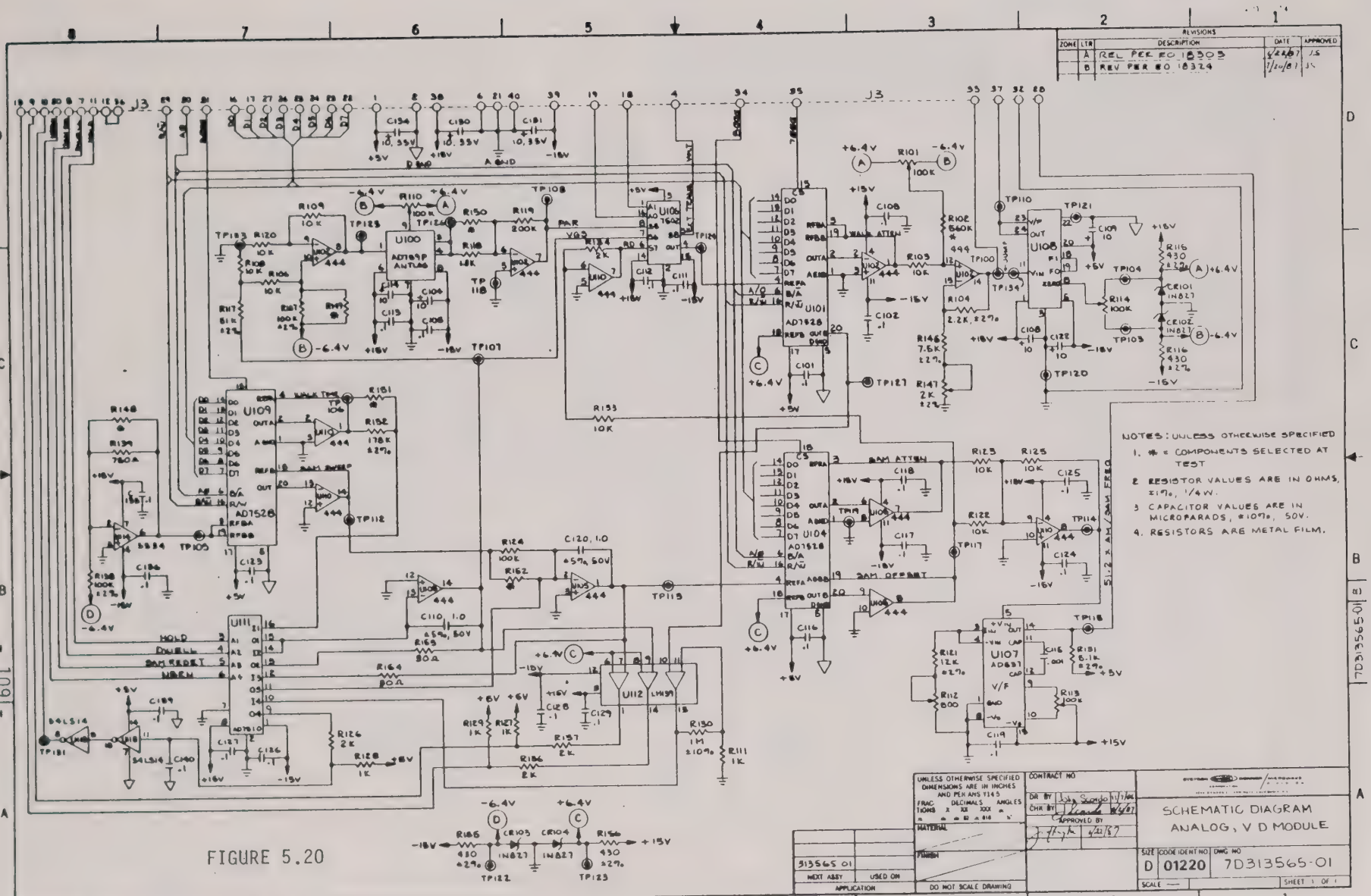
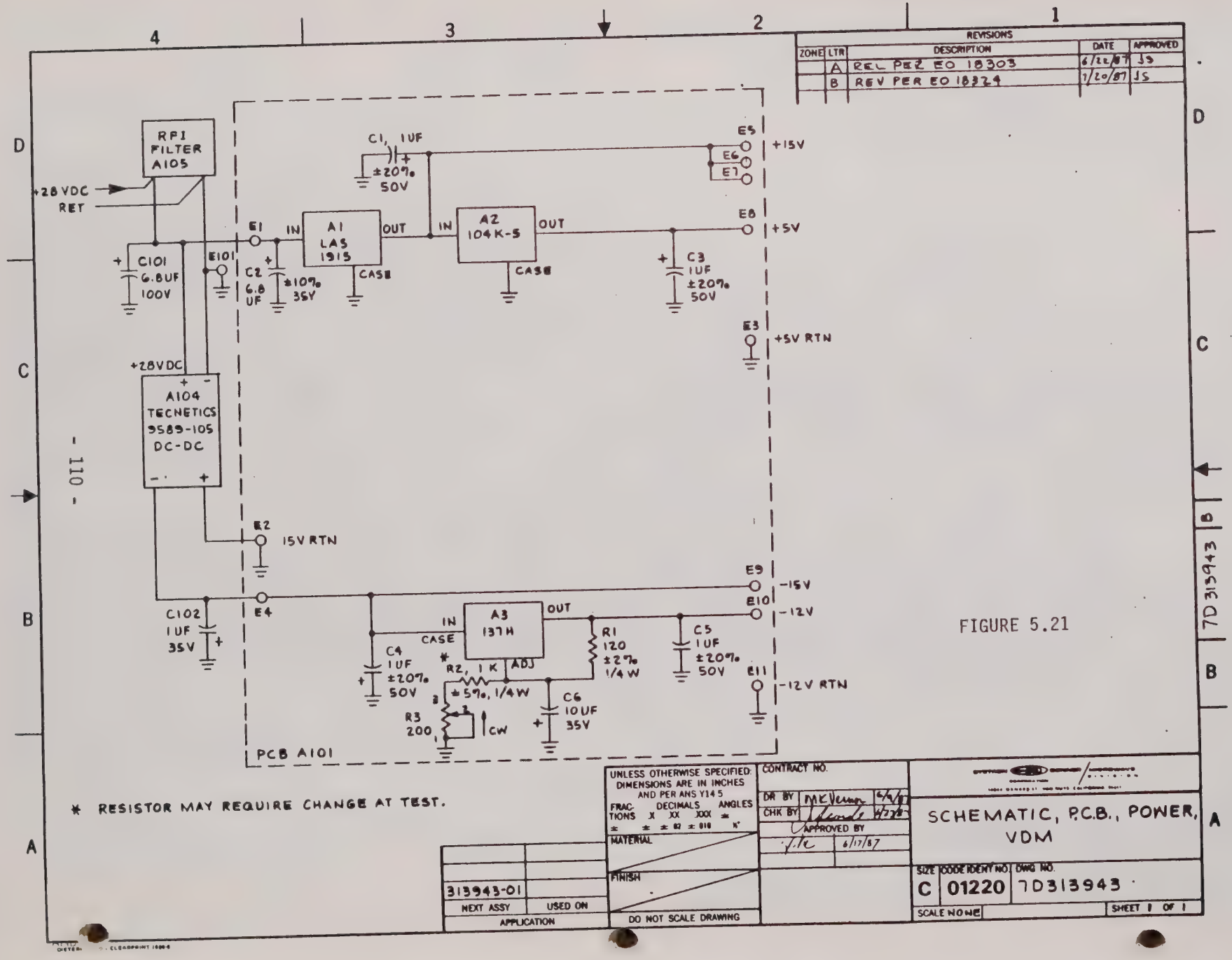

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REL PER EO 18303 | 6/24/87 | JS
B | REV PER EO 18324 | 7/20/87 | JS
NOTES: UNLESS OTHERWISE SPECIFIED
1. * = COMPONENTS SELECTED AT TEST
2. RESISTOR VALUES ARE IN OHMS, ±1%, 1/4W.
3. CAPACITOR VALUES ARE IN MICROPARADS, ±10%, 50V.
4. RESISTORS ARE METAL FILM.
SCHEMATIC DIAGRAM
ANALOG, V D MODULE
7D313565-01
SIZE D
CODE IDENT NO 01220
SHEET 1 OF 1
DO NOT SCALE DRAWING
313565 01
NEXT ASSY
USED ON
APPLICATION
U100 AD7893P ANTLOG
U101 AD7528
U104 AD7528
U107 AD681
U108 AD7893P LOG
U109 AD7528
U111 AD7810
U112 LM139
J3
TP100
TP101
TP102
TP103
TP104
TP105
TP106
TP107
TP108
TP109
TP110
TP111
TP112
TP113
TP114
TP115
TP116
TP117
TP118
TP119
TP120
TP121
TP122
TP123
TP124
TP125
TP126
TP127
TP128
TP129
TP130
TP131
+15V
+6.4V
-6.4V
-15V
+5V
+18V
-18V
A GND
D GND

FIGURE 5.20


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REL PER EO 18303 6/22/87 JS
B REV PER EO 18324 7/20/87 JS
RFI FILTER A105
+28 VDC
RET
C101 6.8UF 100V
E101
E1
C2 6.8 UF ±10% 35V
A1 LAS 1915
IN
OUT
CASE
C1, 1UF ±20% 50V
A2 104K-5
C3 1UF ±20% 50V
E5
E6
E7
+15V
E8
+5V
E3
+5V RTN
+28VDC
A104 TECNETICS 9589-105 DC-DC
E2
15V RTN
C102 1UF 35V
E4
E9
-15V
E10
-12V
A3 137H
C4 1UF ±20% 50V
*R2, 1K ADJ ±5%, 1/4W
R3 200
CW
C6 10UF 35V
R1 120 ±2% 1/4W
C5 1UF ±20% 50V
E11
-12V RTN
PCB A101
- 110 -
7D313943 B
* RESISTOR MAY REQUIRE CHANGE AT TEST.
FIGURE 5.21
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND PER ANS Y14.5
FRACTIONS DECIMALS ANGLES
CONTRACT NO.
DR BY MK Vernon 6/17/87
CHK BY 6/17/87
APPROVED BY 6/17/87
MATERIAL
FINISH
DO NOT SCALE DRAWING
313943-01
NEXT ASSY USED ON
APPLICATION
SCHEMATIC, P.C.B., POWER, VDM
SIZE C
CODE IDENT NO. 01220
DWG NO. 7D313943
SCALE NONE
SHEET 1 OF 1

6.0 Maintenance

6.0.1 Preventative Maintenance:

a) Clean the VDA exterior metal surface using a mild detergent solution.

b) Clean the SMA connectors at J6003 & J6002. Also clean multipins connector J6001 using a Q-Tip dipped in alcohol solution.

6.0.2 Corrective Maintenance:

6.0.2.1 Replace two GaAs Fet Amplifiers A107, A108; one Phase Shifter A106; ±15 V Regulator A1; +5 V Regulator A1; +5 V Regulator A2, Cable Assembly P/N 313567, 312083, 314149, 313568.

a) Remove 22 flathead screws, 2-56 x .25 to open the top cover (see Figure 6.0.2.1)

b) To replace A1 or A2 Regulator, simply loosen the two panhead screws, 6.32 x .50 to remove and replace these components.

c) Loosen the two nuts at RF input and output SMA connectors.

d) Remove the 12 Phillips-head screws that secure the A107, A108 assemblies and carefully lift up the entire assembly from RF input and output port.

e) Remove the Allen screws at the input and output ports of A106, A107 and A108.

f) Unsolder the wires at A106, A107 or A108 that need to be replaced.

g) Install the Allen screws to secure the cable assemblies. to A106, A107 and A108.

h) Carefully re-install the entire assembly back to the VDA housing RF input and output port. Install the Phillips-head screws to secure A106, A107 and A108 assemblies to the VDA housing.

i) Install the two nuts at RF input and output SMA connectors

j) Re-install the 22 flathead screws to secure the top cover to the VDA housing.

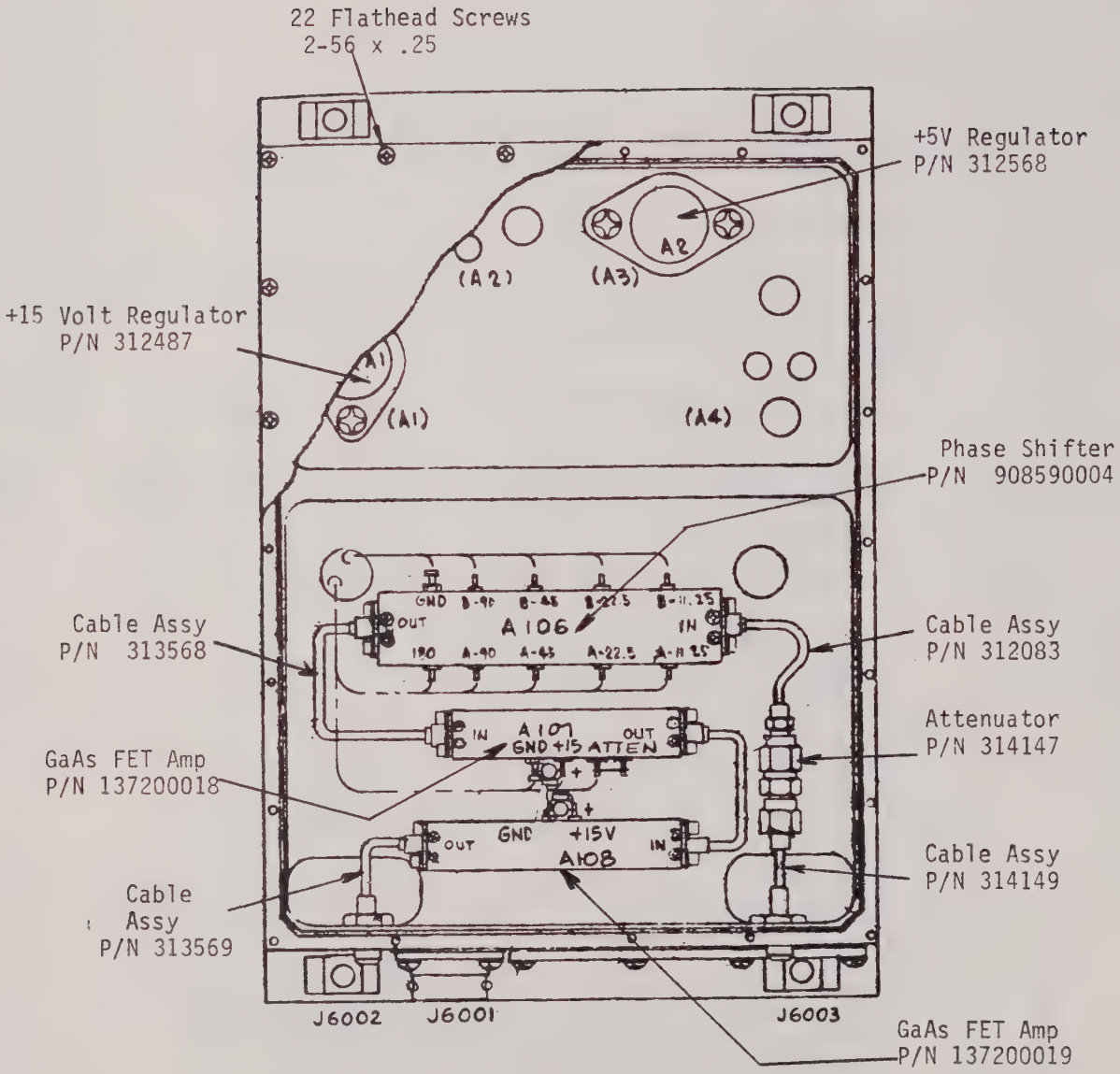
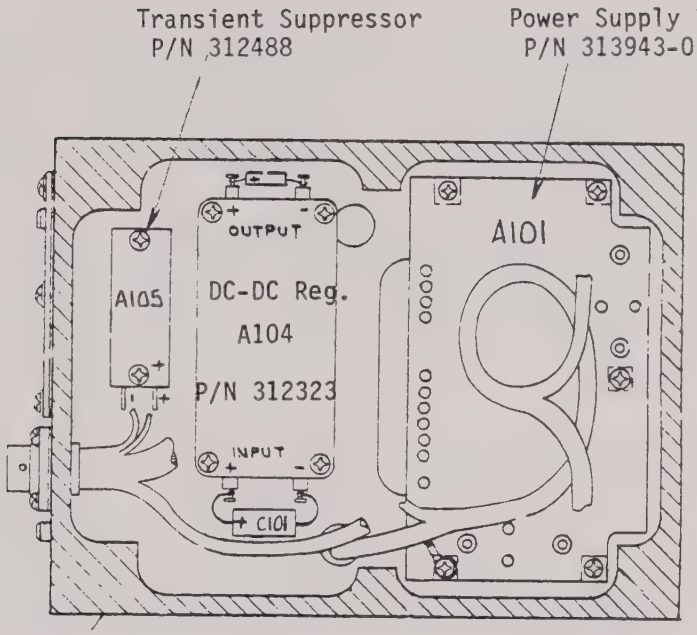


Figure 6.0.2: Detailed VDA Assembly for Corrective Maintenance



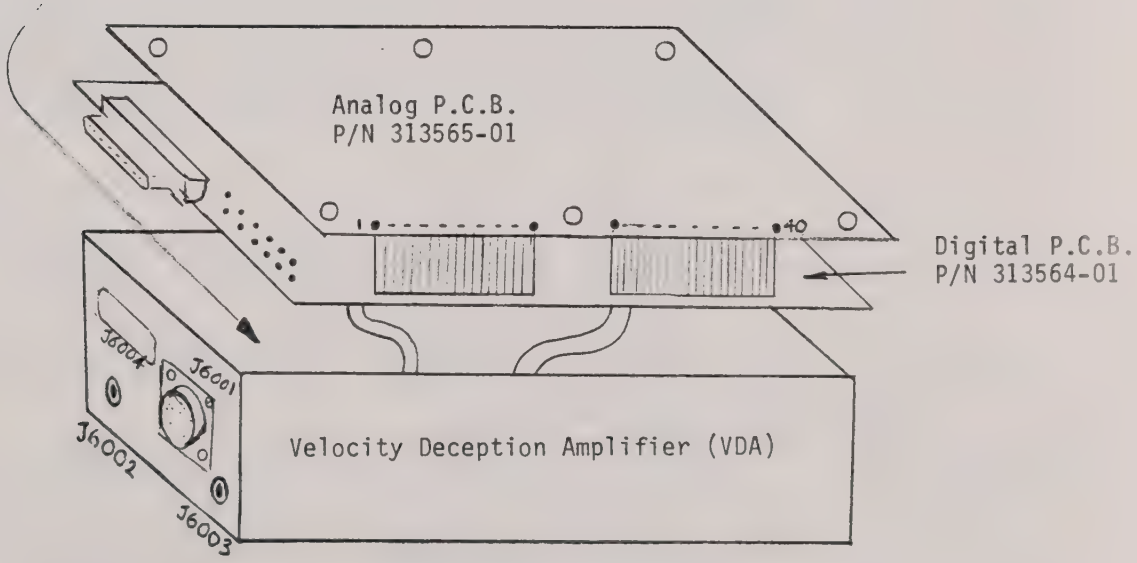


Figure 6.0.3: Detailed VDA Assembly for Corrective Maintenance

6.0.2.2 Replace components on digital/analog A102, A103, PCB, power supply A101 PCB, -15 Regulator A104 and A105.

a) Remove the 22 flathead screws that secure the base cover to the VDA housing. (See Figure 6.0.2.2)

b) Remove the six Phillips-head screws that secure the digital/analog PCB assembly A102, A103 to the VDA housing.

c) Lift the A102, A103 assembly from the VDA housing. All PCB and components on this side are now easily accessed for troubleshooting and replacement. Carefully install a piece of cardboard insulation between the bottom of the digital A103 PCB and VDA housing to test A102, A103 PCB assemblies.

d) Remove the four Phillips-head screws and wires at A104 to replace this module.

e) To replace any component such as -12 V Regulator A3 on A101 power supply PCB. Remove the four Phillips-head screws that secure the A101 PCB to the VDA housing. Remove and replace the defective part as necessary and re-install these four Phillips-head screws to secure the A101 PCB to VDA housing.

6.0.3 Calibration

6.0.3.1 General: The VDA is a microporcessor-based, solid state EW subsystem. Most VDA parameters are set and programmable via microcomputer hardware and software. Therefore, minimum calibrating adjustments are required to perform the VDA calibration. The following are the VDA sections requiring yearly calibration:

a) Power Supply Section.

b) The VGS walktime; minimum and maximum deviation on both linear and parabolic function.

c) The MFR and RSAM frequency; RSAM sweep time.

6.0.3.2 Power Supply Calibration:

a) Follows paragraph 6.0.2.2 for corrective maintenance.

b) Turn the +28 $\pm$ 3 VDC power supply on. Check the test points on power supply PCB A101 with a DVM as follows on next page:

Parameter Tested		Acceptance Limits	Calibration Remarks
E1 (+)	E2 (-)	+28 ± 3 Vdc	Power Supply Input
E5 (+)	E3 (-)	+15 Vdc ± 500 mV	No adjustment necessary
E6 (+)	E3 (-)	+15 Vdc ± 500 mV	No adjustment necessary
E7 (+)	E3 (-)	+15 Vdc ± 500 mV	No adjustment necessary
E8 (+)	E3 (-)	+5 Vdc ± 50mV	No adjustment necessary
E9 (+)	E11 (-)	-15 Vdc ± 500 mV	Adjust pot "INC" at A104 module as necessary
E4 (+)	E11 (-)	-15 Vdc ± 500 mV	Adjust pot "INC" at A104 module as necessary
E4 (+)	E11 (-)	-12 Vdc ± 500 mV	Adjust pot R3 or re-select R2 on A101 PCB as necessary

6.0.3.3 VGS Mode Calibration:

a) Remove the 22 flathead screws that secure the base cover to the VDA housing. All adjustments for the VGS mode are on the component side of the Analog PCB A102.

b) Turn to + 28 Vdc power supply on. Set the VDA parameters via data entry module (DEM). Monitor the VGS test points on the oscilloscope and perform the calibration as follows:

	Parameter Tested	Test Points	Parameter Entry	Acceptance Limits	Calibration Remarks
*	VGS Linear/Parabolic Walk Time	TP124	0.1 secs.	0.1 sec. ± 10%	Re-select R151 as necessary
	VGS Linear/Parabolic Walk Time	TP124	.5 secs.	5 secs ± 10%	Re-select R151 as necessary
	VGS Linear/Parabolic Walk Time	TP124	25.5 secs.	25.5 secs. ± 5%	Use stopwatch as necessary
*	VGS Linear/Parabolic Dwell Time	TP124	0.05 secs.	0.05 secs. ± 10%	No adjustment necessary
	VGS Linear/Parabolic Dwell Time	TP124	5.0 secs.	5.0 secs. ± 5%	No adjustment necessary
*	VGS Linear Max. Freq. Translation	J6002	500 Hz	500 Hz ± 10%	Re-adjust pot. R101 or re-select R102 as necessary
	VGS Linear Max. Freq. Translation	J6002	127.5 KHz	127.5 KHz ± 5%	Re-adjust pot. R147 as necessary

	Parameter Tested	Test Points	Parameter Entry	Acceptance Limits	Calibration Remarks
	VGS Linear Max. Freq. Translation	J6002	5 KHz	5 KHz ± 5%	No adjustment necessary
	SERRO WFM	J6001-10	f = 5 KHz walk = 1 sec. dwell = 5 secs.	<100 Hz	Adjust pot. R114 as necessary
*	VGS Parabolic Max. Freq. Translation	J6002	500 Hz	500 Hz ± 10%	Adjust pot. R110 as necessary
*	VGS Parabolic Max. Freq. Translation	J6002	127.5 KHz	127.5 KHz ± 5%	Re-select R150 as necessary
	AM WFM	J6001-11	10 Hz	10 Hz ± 10%	Re-adjust pot. R113 as necessary
	AM WFM	J6001-11	2550 Hz	2550 Hz ± 5%	Re-adjust pot. R112 as necessary
	Duty Cycle	J6001-11	10%	10%	No adj. necessary
	Duty Cycle	J6001-11	90%	90%	No adj. necessary

6.0.3.5 RSAM Mode Calibration:

RSAM WFM	J6001-12	SAM BEG = 5Hz SAM END = 1275 Hz	+6.4 V	No adj. necessary
	J6001-11	SAM BEG = 5Hz SAM END = 5 Hz	5 Hz ± 10%	Re-adjust pot. R113 as necessary
	J6001-11	SAM BEG = 1275 Hz SAM END = 1275 Hz	1275 Hz ± 5%	Re-adjust pot. R112 as necessary

7.0 REPLACEABLE PART LIST

REPLACEABLE PART LIST FOR VDA #1611AS722

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
VDA	312068-01	Same	Solid State Velocity Deception Amplifier	1
	WL 312068-01	Same	Wire List	1
A101	313943-01	Same	P.C.B. Assy. Power	1
A102, A103	313571-01	Same	P.C.B. Digital/Analog	1
A104	312323	Comp. Prod. #9589-105	DC-DC Regulator	1
A105	312488	Gen. Semi #704-15K36	Filter, Suppressor	1
A106	908590004	Same	Phase Shifter, 5-Bit	1
A107	137200018	Same	Gas FET Amp. Assy., Input	1
A108	137200019	Same	Gas FET Amp. Assy., Output	1
	* 312054	Same	Assy., Data Entry Module	1
	* 314072	Same	Assy., Interface Module	1
	313566	Same	Main Housing	1
	312077	Same	Base Plate	1
	312078	Same	Cover	1
	313513	Same	Access Cover Plate	1
	313514	Same	Gasket, Access Cover	1
	313567	Same	Cable Assembly	1
	312083	Same	Cable Assembly	1
	314149	Same	Cable Assembly	1
	313568	Same	Cable Assembly	1
	313570	Same	Hardness Assy. I/O	1
	312371	Same	Gasket Connector	1

* Optional Items :	312054	Data Entry Module	1
	314072	RS232 Interface Module	1

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
	314050	Same	Hardness Assy., Power	1
	314147	EMC #4402	Attenuator, Fixed 2 dB	1
A1	312487	Lambda #LAS1915	Voltage Regulator +15 V	1
A2	312568	Nat. Sem. #LM140K-5	Voltage Regulator +5 V	1
C101	312489		Cap. Tant. 6.8 { F, 100 V	1
C102	100082		Cap. Tant., 1 { F, 35 V	1
C103, C105	107041		Cap. Tant. 10 { F, 20 V	2
C104, C106	310699		Cap. .1 { F, 100 V	2
	311375		Gasket (‖ 56")	1
E101	108100		GRD LUG, N.4	1
	10063208		Screw Pan HD 6-32 x .50	4
	10062616		Screw Pan HD 2.20 x 1.0	10
	10062612		Screw Pan HD 4.40 x 0.75	2
	10062602		Screw Pan HD 2-56 x 0.375	15
	10062506		Screw Pan HD 2-56 x .375	12
	MS16995-1		Screw Soc. HD 2-56 x .187	12
	10070004		Screw Flat HD, 100°, 2-56 x .25	44
	107376	NAS620-2	Washer, Flat, #2	12
	100712		Washer, Lock, #6	4
	110711		Washer, Lock, #4	27
	108673	MS35338-134	Washer, Lock, #2	14
	314051		ID Plate	1

REPLACEABLE PART LIST FOR VDA INTERFACE MODULE ASSY

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
	314072	Same	Interface Module Assy.	1
	WL314072	Same	Wire List	1
	314073-001	Same	Assy., Interface P.C.B.	1
	314074-001	Same	Assy., Switch P.C.B.	1
	314075	Same	Housing	1
	314076	Same	Base Plate	1
	314077-01	Same	Support P.C.B.	1
	314078	Same	Retainer P.C.B.	1
	314079	Same	Cover, Switch Access	1
	314082	Same	Gasket Switch Access	1
	314081	Same	Cable Assy.	1
	314083	Same	Gasket, Output Conn	1
	311375	Same	Gasket	1
	Same	MS3120E14-19P	Conn., Circ. FLG MTC, RCPT, 19 pins	1
	Same	MS3134E19-4P	Conn., Circ., JN MTG, RCPT 4 pins	1
	Same	M24308/4-304	Conn., D, FL MTG, PLUG, 25 pins	1

REPLACEABLE PART LIST - POWER SUPPLY PCB #313943

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
	313943-01		Power Supply PCB Assy.	1
A3	312845	LM137HVH	Voltage Regulator	1
C1, 3, 4, 5	M39003/01-2357	Same	Cap. Tant., 1 mf, 50 V, ± 20%	4
C2	M39003/01-2304	Same	Cap. Tant., 6.8 mf, 35 V, ±10%	1
C6	M39003/01-2374	Same	Cap. Tant., 10 mf, 50 V, ±10%	1
R1	RCR07C1200GM	Same	Resistor 120 1/4 W, ± 2%	1
R2	RLR07C1101JM	Same	Resistor 11 K, 1/4 W, ± 5%	1
R3	101946	Same	Potentiometer, 200 Ω 20 T, ± 10%, 1/4 W	1

REPLACEABLE PART LIST, ANALOG PCB

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
A102	313565-01	Same	Analog PCB Assy	1
U102, 105, 110	312291	Nat. Sem. LF444AM	I.C. Low Noise Op. Amp.	3
U114	312574	Sig. SE5534AN	I.C. Low Noise Op. Amp.	1
U112	312292	Nat. Sem. LM139	I.C. Quad Comparator	1
U101, 104, 109	312294	Anal. Dev. AD7528TD	I.C. D/A Converter	3
U111	312299	Anal. Dev. AD7510D1BD	I.C. Multiplexer	1
U106	312293	Anal. Dev. AD7502SD	I.C. Multiplexer	1
U118	313692	Any 54LS14J	I.C. Schmitt Trigger	1
U100	310376	Anal. Dev. AD759P	I.C. Log Amp.	1
U107	410265	Anal. Dev. AD537SD	I.C. V/F Converter	1
U108	313623	Dymec 7568	I.C. V/F Converter	1
R103, 106, 108, 109, 120, 122, 123, 123, 133	RLR07C 1002 FM	Same	Resistor, M.F., 10K, ± 1%, 1/4 W	9
R107, 138, 124	RLR07C 1003GM	Same	Resistor M.F., 100K, ± 1%, 1/4 W	3
R146	RLR07C 7501GM	Same	Resistor M.F., 7.5K, ± 1%, 1/4 W	1
R126, 134, 136, 137	RLR07C 2001FM	Same	Resistor M.F., 2K, ± 1%, 1/4 W	4

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
R118	RLR07C 1801FM	Same	Resistor M.F., 1.8K ± 1%, 1/4 W	1
R111, R127, 126, 129	RLR07C 1001GM	Same	Resistor M.F.,1K, ± 1%, 1/4 W	4
R104	RLR07C 2201GM	Same	Resistor M.F., 2.2K, ± 2%, 1/4 W	1
R131	RLR07C 5101GM	Same	Resistor M.F., 5.1K, ± 2%, 1/4 W	1
R132	RLR07C 1783GM	Same	Resistor M.F., 178K, ± 2%, 1/4 W	1
R119	RLR07C 2003GM	Same	Resistor M.F., 200K, ± 2%, 1/4 W	1
R153, 154	RLR07C 30R0FM	Same	Resistor M.F., 30 Δ ± 1%, 1/4 W	2
R139	RLR07C 7500GM	Same	Resistor M.F., 750 Δ ± 2%, 1/4 W	1
R115, 116, 155, 156	RLR07C 4300GM	Same	Resistor M.F., 430 Δ ± 2%, 1/4 W	4
R121	RLR07C 1202GM	Same	Resistor M.F., 12K, ± 2%, 1/4 W	1
R117	RLR07C 5102GM	Same	Resistor M.F., 51K, ± 2%, 1/4 W	1
R130	RN55D104F	Same	Resistor M.F., 1M, ± 5%, 1/8 W	1
R101, 110, 113, 114	102162	Same	Potentiometer, 20T, 100K, ± 10%, 1/4 W	4
R112	107544	Same	Potentiometer, 500 Δ 100K, ± 10%, 1/4 W	1
R147	107276	Same	Potentiometer, 2K 100K, ± 10%, 1/4 W	1

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
C101, 102, 103, 105, 111, 112, 113, 116, 117, 118, 119, 123, 124, 125, 126, 127, 128, 129, 135, 136, 139, 140	M39014/01-1513	Same	CAP.C. Mold .1MF, ± 10%, 50 V	22
C115	M39014/01-1317	Same	CAP.C. Mold .001 MF, ± 10%, 200 V	1
C104, 108, 109, 114, 122, 130, 131, 134	107446	Same	CAP. Tant. 10 MF, ± 10% 35 V	8
C110, 120	312575	Same	CAP, Polycarb, 1 MF, ± 2%, 50 V	2
CR101, 102, 103, 104	100386	Same	Diode, Zener, 6.2 V	4

REPLACEABLE PART LIST FOR DIGITAL PCB

Reference Designation	Systron Donner P/N	Mfg. P/N	Name of Component & Description	Qty.
A103	313564-01	Same	Digital PC Assy	1
U1	312305	Mot. MC68 9BQCA	I.C. C.P.U. 8-Bit	1
U2	312306	Intel. M2764A-35	I.C. 8K x 8 EPROM	1
U3, U6	410402	XICOR X2212DM	I.C. NOVRAM	2
U4, U7	312308	Harris 6561B-2	I.C. 1K RAM	2
U10, 11	312286	Any. 54LS191J	I.C. U/D Counter	2
U14, 19	312309	Mot. MC6840BICA	I.C. Timer	2
U5, 8, 12, 17, 22, 23, 24, 25, 26	313622	NEM. 261-83B	I.C. Pin Diode Driver	9
U9	312601	Any. 54154J	I.C. Decoder	1
U113	312287	Any. 54365J	I.C. Hex/Buffer Driver	1
U15	312282	Any. 5474J	I.C. D Flip Flop	1
U16, 29	311681	Any. 54LS86J	I.C. XOR Gate	2
U18	312281	Any. 5400J	I.C. Quad. NAND Gate	1
U20	312288	Any. 54377J	I.C. D Flip Flop	1
U21	312284	Any. 54153J	I.C. Line Data Selector	1

Reference Designation	Systron Donner P/N	MFG P/N	Name of Component & Description	Qty.
U27, 28	313691	Any. 54164J	I.C. Shift Register	2
Y1	312576	Monitor Prod. MC18A - 4.0 MHz	XTAL, 4 MHz	1
CR1, CR2	107042	1N941	Diode	2
Q1	113351	2N2222A	Transistor	1
R1, 2, 3, 4, 5, 6, 7, 8, 13	RLR07C 1500GM	Same	Resistor M.F., 150 Δ ± 2%, 1/4 W	9
R9, 10, 11	RLR07C 5100GM	Same	Resistor M.F., 510 Δ ± 2%, 1/4 W	3
R12	RLR07C 1000FM	Same	Resistor M.F., 100 Δ ± 1%, 1/4 W	1
R14, 17	RLR07C 1001FM	Same	Resistor M.F., 1K ± 1%, 1/4 W	2
R15	RLR07C 3301GM	Same	Resistor, M.F., 3.3K, ± 2%, 1/4 W	1
R16	104890	Same	Resistor, M.F., 10 Δ ± 2%, 1 W	1
RP1	410049	4308R-101-103	Resistor Network SIP, 10K, ± 2%, 1 W	1
RP2	312494	4308R-101-332	Resistor Network SIP, 3.3K, ± 2%, 1/4 W	1
RP3	410051	4310R-101-332	Resistor Network, SIP, 3.3 K, ± 2%, 1/4 W	1
C1, 15, 23, 28, 45	107446	196D106X90 35LA3	Cap. Tant., 10 mF, 10%, 35 v	5
C3	312504	T363C68 6K015AS	Cap. Tant., 68 mF, 10%, 15 v	1